L79 ANSWER 10 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1999-396228 [34] WPIX
DNN N1999-296237
TI Lateral high voltage transistor - has **trenches** in **epitaxial** layer in rows and columns between source and drain electrodes with **walls doped** with **dopant** of first conductive type.
DC U12
IN TIHANYI, J
PA (SIEI) SIEMENS AG
CYC 20
PI DE 19828191 C1 19990729 (199934)* 4p H01L029-78
WO 9967826 A1 19991229 (200008) DE H01L029-06
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: JP US
EP 1008184 A1 20000614 (200033) DE H01L029-06
R: DE FR GB IE IT
US 6326656 B1 20011204 (200203) H01L029-72
JP 2002519852 W 20020702 (200246) 9p H01L029-78
ADT DE 19828191 C1 DE 1998-19828191 19980624; WO 9967826 A1 WO 1999-DE761 19990317; EP 1008184 A1 EP 1999-913117 19990317, WO 1999-DE761 19990317; US 6326656 B1 Cont of WO 1999-DE761 19990317, US 2000-511813 20000224; JP 2002519852 W WO 1999-DE761 19990317, JP 2000-556403 19990317
FDT EP 1008184 A1 Based on WO 9967826; JP 2002519852 W Based on WO 9967826
PRAI **DE 1998-19828191 19980624**
IC ICM H01L029-06; H01L029-72; H01L029-78
AB DE 19828191 C UPAB: 19990825
The lateral high voltage transistor has a semiconductor body (1,2). The semiconductor body has a weakly **doped** semiconductor substrate (1) of a first conductive type. An **epitaxial** layer (2) of the opposite conductive type is provided on the semiconductor substrate (1).
The transistor also has a drain electrode (3), a source electrode (5) and a gate electrode (7). A semiconductor **zone** (4) of the first conductive type is provided under the gate electrode (7) and is embedded in the **epitaxial** layer (2). **Trenches** (8) are provided in the **epitaxial** layer (2) arranged in rows and columns between the source electrode (5) and the drain electrode (3). The **walls** of the **trenches** (8) are highly **doped** with **dopant** of the first conductive type.
USE - Transistor is used for HV-FET. LIGBT.
ADVANTAGE - Transistor has structure which can be manufactured in relatively simple manner.
Dwg.1/2
FS EPI
FA AB; GI

L48 ANSWER 1 OF 10 WPIX (C) 2002 THOMSON DERWENT
AN 2000-648367 [63] WPIX
DNN N2000-480604
TI Minority charge carrier injection prevention circuit for integrated semiconductor circuit - has switch controlled by potential at circuit output and connected between circuit output and substrate terminal.
DC U11 U13 U24
IN FELDTKELLER, M; TIHANYI, J
PA (SIEI) SIEMENS AG; (SIEI) INFINEON TECHNOLOGIES AG
CYC 25
PI DE 19928762 C1 20001123 (200063)* 8p H01L023-58
EP 1063703 A1 20001227 (200102) DE H01L027-02
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
ADT DE 19928762 C1 DE 1999-19928762 19990623; EP 1063703 A1 EP 2000-111573 20000530
PRAI **DE 1999-19928762 19990623**
IC ICM H01L023-58; H01L027-02
ICS H01L027-08
AB DE 19928762 C UPAB: 20001205
The circuit for preventing injection of minority charge carriers in an IC semiconductor substrate uses at least one switch (S1,S3) connected between an output terminal (A1,A3) and a substrate terminal (SUB) of the semiconductor circuit, controlled in dependence on the potential at the output terminal.

The control circuit (AS) for the latter switch(es) may also control a further switch (S2) connected between a reference potential (M) and the substrate terminal, e.g. in parallel with a resistance (Rsub).

USE - Circuit is used for preventing injection of minority charge carriers for integrated circuit substrate.

ADVANTAGE - Circuit blocks pn-junction with substrate at high voltage difference between output and substrate.
Dwg.2/3
FS EPI

L79 ANSWER 25 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1994-084797 [11] WPIX
DNN N1994-066380
TI Power MOSFET with cells connected in parallel - has ring-shaped zone with annular trench lying between cells and edge of semiconductor body.
DC U12
IN HERTRICH, H
PA (SIEI) SIEMENS AG
CYC 19
PI EP 586716 A1 19940316 (199411)* DE 5p H01L029-784
R: AT BE CH DE DK ES FR GB GR IE IT LI LU MC NL PT SE
JP 06169090 A 19940614 (199428) 4p H01L029-784
US 5418394 A 19950523 (199526) 6p H01L029-784
EP 586716 B1 19971022 (199747) DE 6p H01L029-772
R: DE FR GB IT
DE 59208987 G 19971127 (199802) H01L029-772

AB EP 586716 A UPAB: 19940428
Inbetween the cells (2) and the edge (13) of the semiconductor body (1) is a ring-shaped zone (14) of same conductivity type as the gate zone (9). The ring-shaped zone has the same depth and doping as the gate zone.

The ring-shaped zone has a ring-shaped trench (5) with the same depth as the contact holes (3), and which is contact by the metal layer (6). The volume of the ring shaped zone which lies between the trench and the edge of the semiconductor body is **free** of the conductivity type of the source zones (10,20).

ADVANTAGE - Has improved avalanche stability, and is more simply produced.
Dwg.1/3

ABEQ US 5418394 A UPAB: 19950705
THe power MOSFET has a cell field in which the lateral cells are provided with source zones which are partly omitted or of a reduced size. A p-doped annular zone is disposed between the cell field and the edge of the semiconductor body. An annular trench is formed in the annular zone.

The annular trench is contacted with the source metallization. The annular zone and the annular trench have the same depth as the gate zones of the cells and/or as the source contact holes.

ADVANTAGE - Improved avalanche resistance.
Dwg.2/3

ABEQ EP 586716 B UPAB: 19971125
Power MOSFET, having a multiplicity of cells which are arranged on a semiconductor body, are connected in parallel and each comprise a gate zone and a source zone embedded therein in a planar manner, having an annular zone which is of the conduction type of the gate zones, surrounds the cells and has the same depth and doping as the gate zones, having a metal layer which makes contact with the gate zones, the source zones and the annular zone, and also having gate electrodes which are connected in parallel with one another, characterized by the features: (a) the metal layer (6) makes contact with the gate zones (9) through contact holes (3) made in the source zones (10), (b) the annular zone (4) has an annular trench (5) having the same depth as the contact holes (3), (c) the metal layer makes contact with the annular zone (4) in the annular trench (5), (d) the semiconductor body is covered with an insulating layer (12) between the annular trench and the edge (13) of the semiconductor body, (e) a conductive layer (8) which is applied at the same time as the gate electrodes is arranged on the insulating layer, (f) that part of the annular zone (4) which lies between the trench (5) and the edge (13) of the semiconductor body is **free** of zones corresponding to the conduction type of the source zones (10,20).
Dwg.1/3
FS EPI

L23 ANSWER 8 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 1989-115414 [16] WPIX
DNN N1989-087985
TI Asymmetrical thyristor with two-layer base zone - has auxiliary thyristor for ignition intensifying, coupled in front of asymmetrical thyristor.
DC U12 U21
IN VOSS, P
PA (SIEI) SIEMENS AG
CYC 1
PI DE 3732210 A 19890413 (198916)* 6p <--
ADT DE 3732210 A DE 1987-3732210 19870924
PRAI DE 1987-3732210 19870924
IC H01L029-74; H03K017-72
AB DE 3732210 A UPAB: 19930923

A first base zone of a first conductivity consists of a lightly doped layer (1) and a heavily doped layer (2). The latter comprises heavily doped regions (3) of a second conductivity, forming a first emitter zone of a reduced depth. A first emitter electrode (4) connects the heavily doped base layer and the emitter zone, while a second base zone (5) of a second conductivity is adjacent to the outer surface of the lightly doped layer.

An auxiliary thyristor for ignition intensifying is coupled in front of the main thyristor. Between the thyristor electrode and a second emitter electrode (7) is incorporated a diode (17) in the same parallel sense, with a lower threshold voltage than the pn-junction between the second emitter zone (6) and the second base zone. A capacitor (16) is in parallel to the diode.

ADVANTAGE - High du/dt strength, high max. operating temp., and improved ignition propagation.

2/6

FS EPI
FA AB; GI

L48 ANSWER 2 OF 10 WPIX (C) 2002 THOMSON DERWENT
AN 1997-054964 [06] WPIX
DNN N1997-045050
TI High voltage integrated circuit for controlling and driving power device - has N channel transistor to shift signal levels from low potential side low voltage circuit to high potential side low voltage circuit with loop shaped high voltage junction terminating structure.
DC U13
IN FUJIHIRA, T
PA (FJIE) FUJI ELECTRIC CO LTD
CYC 8

PI	EP 751572	A2 19970102	(199706)*	EN	21p	H01L027-02
	R: CH DE FR GB LI NL					
	JP 09074198	A 19970318	(199721)		13p	H01L029-78
	US 5736774	A 19980407	(199821)		19p	H01L029-00
	JP 3228093	B2 20011112	(200174)		10p	H01L029-78
	JP 2002026708	A 20020125	(200211)		10p	H03K017-10
	JP 2002026714	A 20020125	(200211)		11p	H03K019-0175

ADT EP 751572 A2 EP 1996-304747 19960627; JP 09074198 A JP 1995-258472 19951005; US 5736774 A US 1996-670601 19960626; JP 3228093 B2 JP 1995-258472 19951005; JP 2002026708 A Div ex JP 1995-258472 19951005, JP 2001-123761 19951005; JP 2002026714 A Div ex JP 1995-258472 19951005, JP 2001-123762 19951005
FDT JP 3228093 B2 Previous Publ. JP 09074198
PRAI **JP 1995-258472 19951005; JP 1995-162139 19950628**
REP No-SR.Pub
IC ICM H01L027-02; H01L029-00; H01L029-78; H03K017-10; H03K019-0175
ICS H01L021-8234; H01L027-088; H01L029-40; H01L029-76; H01L029-94; H03K017-687; H03K019-018
AB EP 751572 A UPAB: 19970205
The IC includes a low potential side low voltage circuit portion and a high potential side low voltage circuit portion, each being supplied by current from a low voltage source having a reference potential point based respectively on the low potential side of a HV source and on one of the main terminals of the power device.

The two circuits are sepd. by a loop shaped HV junction terminating structure [HVJT]. A HV n-channel transistor for level shifting signals from the low to the HV circuit, has its drain located inside another loop shaped HV junction terminating structure and its source and gate outside it. Signal wiring from the drain to the high potential side low voltage portion is spaced apart from the junction terminating structures.

ADVANTAGE - HV device with HV level shift unit having reduced mfg. cost.

Dwg.1a/11
FS EPI

L23 ANSWER 9 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 1986-266140 [41] WPIX
DNN N1986-198897
TI Integrated circuit for control of inductive load - has vertical transistor inbuilt diode and Zener diode acting as damping diodes.
DC U13 V02 V03
IN ERRATICO, P; MARCHIO, F; MENNITI, P
PA (SGSA) SGS MICROELETTRONICA SPA; (SGSA) SGS ATES COMPONENTI ELTRN SPA
CYC 4
PI DE 3609629 A 19861002 (198641)* 12p <--
FR 2579830 A 19861003 (198646)
JP 61231746 A 19861016 (198648)
IT 1221019 B 19900621 (199216)
ADT DE 3609629 A DE 1986-3609629 19860321; JP 61231746 A JP 1986-75374 19860331; IT 1221019 B IT 1985-20174 19850401
PRAI IT 1985-20174 19850401
IC H01F007-18; H01H047-32; H01L027-06; H01L029-90; H03K017-64
AB DE 3609629 A UPAB: 19930922

A vertical p-n-p transistor with insulated collector consists of a p-type substrate (1) with a covering n-type layer (2) covered, in turn, by a p-type layer (3) which forms the collector, both layers being formed by ion implantation. An epitaxial n-type layer (4) encloses the two layers and has n+ (6) regions embedded which form the base and emitter of the transistor respectively. A p+ region (8) links the collector to the external electrode (A).

The two junctions of the floating first layer (2) with the adjacent regions (1,3) form a series connected diode and Zener diode connected effectively in parallel to the load.

ADVANTAGE - Does not require external damping diode.

1/2

L48 ANSWER 3 OF 10 WPIX (C) 2002 THOMSON DERWENT
AN 1993-266100 [34] WPIX
DNN N1993-204103
TI Substrate insulation structure used in integrated circuits - has power supply connected to active element gate terminal with parasitic diodes between drain terminal and source and substrate respectively, so that active element is reverse biased w.r.t. substrate.
DC U11 U12 U13
IN CONSIGLIO, P; ERRATICO, P
PA (SGSA) SGS THOMSON MICROELTRN SRL; (SGSA) STMICROELECTRONICS SRL; (SGSA) SGS THOMSON MICROELTRN SARL
CYC 6

PI	EP 556743	A1	19930825	(199334)*	EN	9p	H01L027-02
	R: DE FR GB						
	JP 06005792	A	19940114	(199407)			H01L027-08
	US 5525832	A	19960611	(199629)		9p	H01L029-10
	IT 1261880	B	19960603	(199705)			H01L000-00
	EP 556743	B1	19990428	(199921)	EN		H01L027-02
	R: DE FR GB						
	DE 69324621	E	19990602	(199928)			H01L027-02

PRAI **IT 1992-MI338 19920217**
REP 01Jnl.Ref
IC ICM H01L000-00; H01L027-02; H01L027-08; H01L029-10
AB EP 556743 A UPAB: 19931119

The insulation structure includes a power supply connected to a terminal (106) of an active integrated element (100) which has with respect to the substrate (104) at least one reverse biased junction (103). The element comprises a DMOS transistor. The source terminal (101) is connected to the drain terminal (102) by a first parasitic diode (103) and the drain terminal (102) is connected to a portion of the substrate by a second parasitic diode (105). The gate (106) is connected to the power supply.

The reverse biased junction comprises the first parasitic diode which is connected with its anode terminal to the source and its cathode terminal to the drain terminal of the DMOS transistor. The gate terminal has a parallel connected protection Zener diode (107).

USE/ADVANTAGE - E.g. telephony circuits. Allows integration of passive and active components.

Dwg.7a/8b

ABEQ US 5525832 A UPAB: 19960724

A current source comprising:

first and second power supply terminals;

an output terminal;

first, second and third bipolar transistors, each transistor having an emitter, collector and base terminal;

at least one diode; and

a switch;

wherein the emitter terminal of the first transistor is connected to the first power supply terminal, the base and collector terminals of the first transistor are connected together, to the base terminal of the second transistor and to the emitter terminal of the third transistor, the emitter terminal of the second transistor is connected to the first power supply terminal, the base terminal of the third transistor is connected through the at least one diode to the switch, the switch is connected to the second power supply terminal, and the collector terminal of the second transistor is connected to the output terminal.

Dwg.7a/8

FS EPI

L48 ANSWER 4 OF 10 WPIX (C) 2002 THOMSON DERWENT

AN 1982-M4340E [38] WPIX

TI Solenoid control circuit - has transistor switch connected in series with solenoid and DC supply terminals and Zener diode.

DC U21 V02 V03

IN BHARJ, B S; SEILLY, A H

PA (LUCA) LUCAS IND LTD

CYC 5

PI	GB 2095065	A	19820922	(198238)*	5p
	DE 3208660	A	19820923	(198239)	
	FR 2501899	A	19820917	(198244)	
	JP 57160103	A	19821002	(198245)	
	IT 1150293	B	19861210	(198842)	

PRAI **GB 1981-7797 19810312; GB 1982-5996 19820302**

IC G05F000-00; H01F007-18; H01H047-02; H02M003-10; H02P007-00; H03K017-04

AB GB 2095065 A UPAB: 19930915

The circuit is for controlling the operation of an electromagnetic device which includes a solenoid and an armature.

It includes a transistor switch (13) connected in series with the solenoid (12) and the d.c. supply terminals, a Zener diode (16) connected in parallel with the switch and a solid state switch with diode and transistor (14,15) connected in parallel with the solenoid. The operation of the switch and the transistor switch are controlled by a control circuit (17).

Switch is opened and solid state switch (14,15) is closed to maintain current flow in the solenoid, the transistor switch being pulsed to maintain an average current flow. When it is required to de-energise the solenoid the switches are both opened and the Zener diode conducts to protect the transistor switch from high voltage induced in the solenoid as well as dissipating the stored energy of the magnetic circuit of the solenoid.

1/4

L23 ANSWER 10 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 1981-H2931D [32] WPIX
TI Monolithic integrated collector-base diode - has emitter zone without galvanic connection to base and collector zones in substrate with epitaxial layer of opposite conductivity.
DC U12
IN JOCHEN, P; KUGELMANN, A
PA (BOSC) BOSCH GMBH ROBERT
CYC 1
PI DE 3002797 A 19810730 (198132)* 9p <--
PRAI DE 1980-3002797 19800126
IC H01L029-86
AB DE 3002797 A UPAB: 19930915

On a semiconductor substrate (1) an epitaxial layer (2) of opposite conductivity is grown. A part of the epitaxial layer, forming the collector zone (3) is separated by insulation diffusion. A base zone (11) is diffused into the collector zone and has the substrate conductivity. An emitter zone (12) of the collector zone conductivity is diffused into the base zone.

This emitter zone has no galvanic connection with the base and collector zones. A highly doped collector terminal zone (13) of the collector conductivity is diffused into the collector zone, and surrounds annularly the base zone. Under the latter is provided a highly doped conductive layer region (16) at the boundary between the substrate and collector zone, having the collector conductivity. The collector terminal zone reaches down to the conductive layer region.

3

FS EPI

L23 ANSWER 6 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 2000-072969 [06] WPIX
DNN N2000-057019
TI Diode device with voltage oscillation suppression due to introduction of a lifetime killer.
DC U11 U12
IN KOGA, S; MORISHITA, K; SATOH, K
PA (MITQ) MITSUBISHI DENKI KK
CYC 21
PI WO 9963597 A1 19991209 (200006)* JA 62p H01L029-861
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: JP US
EP 1026754 A1 20000809 (200039) EN H01L029-861 <--
R: CH DE LI
JP 11535937 X 20010313 (200117) H01L029-861
US 6218683 B1 20010417 (200123) H01L029-74
ADT WO 9963597 A1 WO 1998-JP2427 19980601; EP 1026754 A1 EP 1998-923079 19980601, WO 1998-JP2427 19980601; JP 11535937 X WO 1998-JP2427 19980601, JP 1999-535937 19980601; US 6218683 B1 WO 1998-JP2427 19980601, US 2000-463407 20000201
FDT EP 1026754 A1 Based on WO 9963597; JP 11535937 X Based on WO 9963597; US 6218683 B1 Based on WO 9963597
PRAI WO 1998-JP2427 19980601
IC ICM H01L029-74; H01L029-861
ICS H01L029-32; H01L029-868; H01L031-111
AB WO 9963597 A UPAB: 20000203
NOVELTY - A lifetime killer is selectively introduced into the semiconductor substrate (20) which has a P (1), N- (2) and N+ (3) layers provided. A first area (6) of the N- layer contains the lifetime killer at the highest concentration and a second area (7), annularly surrounding the N- layer, contains a lower concentration. Resulting in carrier lifetimes of the first, second and third areas become longer respectively.
USE - Semiconductor diode manufacture.
ADVANTAGE - The diode can simultaneously realize a high di/dt resistance, a low recovery loss and a low forward voltage. Also the diode can suppress the occurrence of voltage oscillation.
DESCRIPTION OF DRAWING(S) - The figure shows a section through the diode device structure.
P layer 1
N- layer 2
N+ layer 3
First area 6
Second area 7
Substrate 20
Dwg.1/42
FS EPI

L48 ANSWER 7 OF 10 JAPIO COPYRIGHT 2002 JPO
AN 1997-074198 JAPIO
TI HIGH WITHSTAND VOLTAGE IC AND HIGH WITHSTAND VOLTAGE LEVEL SHIFT CIRCUIT USIDED THEREFOR
IN FUJIHIRA TATSUHIKO
PA FUJI ELECTRIC CO LTD
PI JP 09074198 A 19970318 Heisei
AI JP 1995-258472 (JP07258472 Heisei) 19951005
PRAI **JP 1995-162139** 19950628
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1997
IC ICM H01L029-78
ICS H01L029-40

AB PROBLEM TO BE SOLVED: To prevent decrease of withstand voltage due to signal wirings, and realize cost reduction, by constituting the signal wirings which sandwiches high withstand voltage junction terminal structures and are arranged, by using bonding wires.
SOLUTION: High withstand voltage junction terminal structures HVJT are formed in GDU1-GDU3, a high withstand voltage n channel MOSFET (HVN), and a high withstand voltage p channel MOSFET (HVP). The drain electrode DN of the high withstand voltage n channel MOSFET (HVN) is connected with GDU1 through SIN1. The drain electrode DP of the high withstand voltage p channel MOSFET (HVP) is connected with LSU through SOUT1.

L79 ANSWER 58 OF 64 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:626499 HCAPLUS
DN 133:186748
TI MOS-gated device having a buried gate and process for fabricating
IN Kocon, Christopher; Zeng, Jun
PA Intersil Corp., USA
SO Eur. Pat. Appl., 11 pp.
CODEN: EPXXDW
DT Patent
LA English
IC ICM H01L029-78
ICS H01L029-739; H01L029-74; H01L021-336; H01L021-331; H01L021-332
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE	
PI	EP 1033759	A2	20000906	EP 2000-102398	20000203	<--
	EP 1033759	A3	20001122			
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO					
	US 6351009	B1	20020226	US 1999-260411	19990301	
	TW 452890	B	20010901	TW 2000-89102283	20000211	<--
	JP 2000252468	A2	20000914	JP 2000-44636	20000222	<--
	US 2002056871	A1	20020516	US 2001-39319	20011109	<--
PRAI	US 1999-260411	A	19990301 <--			

AB An improved **trench** MOS-gated device comprises a monocryst. semiconductor substrate on which is disposed a **doped** upper layer. The upper layer includes at an upper surface a plurality of heavily **doped** body **regions** having a 1st polarity and overlying a drain **region**. The upper layer further includes at its upper surface a plurality of heavily **doped** source **regions** having a 2nd polarity opposite that of the body **regions** A gate **trench** extends from the upper surface of the upper layer to the drain **region** and separates one source **region** from another. The **trench** has a floor and **sidewalls** comprising a layer of dielec. material and contains a conductive gate material filled to a selected level and an isolation layer of dielec. material that overlies the gate material and substantially fills the **trench**. The upper surface of the overlying layer of dielec. material in the **trench** is thus substantially coplanar with the upper surface of the upper layer. A process for forming an improved MOS-gate device provides a device whose gate **trench** is filled to a selected level with a conductive gate material, over which is formed an isolation dielec. layer whose upper surface is substantially coplanar with the upper surface of the upper layer of the device.
ST MOS device fabrication
IT Electric contacts
Gate contacts

L79 ANSWER 4 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 2000-414714 [36] WPIX
DNN N2000-309876 DNC C2000-125847
TI **Trench** MOSFET is formed in structure that includes a P-type **epitaxial** layer overlying an N+ substrate.
DC L03 U11 U12
IN DARWISH, M; DARWISH, M N
PA (SILI-N) SILICONIX INC
CYC 27
PI EP 1014450 A2 20000628 (200036)* EN 20p H01L029-00
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
JP 2000164869 A 20000616 (200036) 18p H01L029-78
US 6084264 A 20000704 (200036) H01L029-76
ADT EP 1014450 A2 EP 1999-106012 19990325; JP 2000164869 A JP 1999-71596 19990317; US 6084264 A US 1998-200197 19981125
PRAI **US 1998-200197 19981125**
IC ICM H01L029-00; H01L029-76; H01L029-78
ICS H01L021-336; H01L029-94; H01L031-062; H01L031-113; H01L031-119
AB EP 1014450 A UPAB: 20000801
NOVELTY - Second conductivity type **epitaxial** layer with **trench** and overlying first conductivity type semiconductor substrate comprises first conductivity source **region** adjacent top surface of layer and **trench sidewall**, second conductivity type body, and first conductivity type drain **region** between substrate and **trench** bottom. Junction between drain **region** and body lies between substrate and **trench sidewall**.

DETAILED DESCRIPTION - A gate is positioned in the **trench** and is electrically isolated from the **epitaxial** layer by an insulating layer that extends along a bottom and a **side wall** of the **trench**.

At least 75%, preferably at least 90%, of the drain **region** is located directly below the **trench**.

The junction between the drain **region**, whose **doping** concentration is 5 multiply 1015 to 5 multiply 1017 cm-3, and the body is an arc that is concave in the direction towards the drain **region**
.

The MOSFET further includes a threshold voltage adjust implant and a body implant

Preferably, the **epitaxial** layer comprises at least two layers: a first sublayer adjacent the surface of the **epitaxial** layer and a second sublayer between the first sublayer and the substrate and having **doping** concentration different than that of the first sublayer. An interface between the two sublayers intersects the **sidewall** of the **trench**.

INDEPENDENT CLAIMS are given for:
(a) two power MOSFETs; and
(b) a process of fabricating a power MOSFET.

USE - None given.

ADVANTAGE - The MOSFET has reduced threshold voltage and on-resistance and increased punch-through breakdown voltage.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view of a **trench** MOSFET in accordance with the invention.

MOSFET 30
Metal layer 31
N+ substrate 32
N drain **region** 33
P-type **epitaxial** layer 34
P-type body or base 34a
Trench 35
N+ source **region** 36

Polysilicon gate 37
P+ body contact **region** 38
Dwg.3/13

L79 ANSWER 1 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 2002-141580 [19] WPIX
DNN N2002-107070 DNC C2002-043803
TI **Compensation** element used as a MOSFET, JFET, IGBT or Schottky diode has a drift path lead around the side surfaces and the base surface of the trench.
DC L03 U12
IN AHLERS, D; PFIRSCH, F
PA (INFN) INFINEON TECHNOLOGIES AG; (AHLE-I) AHLERS D; (PFIR-I) PFIRSCH F
CYC 27
PI EP 1160871 A2 20011205 (200219)* DE 7p H01L029-06
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
DE 10026924 A1 20011220 (200219) H01L029-06
US 2001048144 A1 20011206 (200219) H01L029-00
ADT EP 1160871 A2 EP 2001-112152 20010517; DE 10026924 A1 DE 2000-10026924 20000530; US 2001048144 A1 US 2001-867502 20010530
PRAI **DE 2000-10026924 20000530**
IC ICM H01L029-00; H01L029-06
ICS H01L021-20; H01L021-306; H01L021-336; H01L029-739; H01L029-78; H01L029-872
AB EP 1160871 A UPAB: 20020321
NOVELTY - **Compensation** element has a drift path between two active zones and a stack of p- and n-conducting regions (3, 4) and a trough-like trench (2). The drift path is lead around the side surfaces and the base surface of the trench.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the production of a **compensation** element comprising:

(a) inserting a trench (2) into a semiconductor body (1) by anisotropic etching;

(b) providing the base surface and the side surfaces with p- and n-conducting layers;

(c) removing the layers on the surface of the semiconductor body in a planarizing step; and

(d) filling the remaining trench on the layers with an insulating material (5) or silicon.

The trench is preferably provided with an oxide filling in addition to the p- and n-conducting regions. The walls of the side surfaces are inclined at 55 deg. .

USE - Used as a MOSFET, JFET, IGBT or Schottky diode (claimed).

ADVANTAGE - The element is easy to manufacture.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section through the **compensation** element.

Semiconductor body 1
Trench 2
p and n conducting regions 3, 4
Insulating material 5
Dwg.4/6
FS CPI EPI

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L79  ANSWER 2 OF 64  WPIX (C) 2002 THOMSON DERWENT
AN   2001-246584 [26]   WPIX
DNN  N2001-175601
TI   An integrated circuit for power applications comprising power and control
     circuit portions incorporated in respective wells separated by a biased
     intermediate region.
DC   U13 X12
IN   AIELLO, N
PA   (SGSA) STMICROELECTRONICS SRL
CYC  26
PI   EP 1049165     A1 20001102 (200126)* EN    11p    H01L027-02
         R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT
            RO SE SI
     US 6337503     B1 20020108 (200211)               H01L031-062
ADT  EP 1049165 A1 EP 1999-830261 19990430; US 6337503 B1 US 2000-560195
     20000428
PRAI EP 1999-830261   19990430
IC   ICM  H01L027-02; H01L031-062
     ICS  H01L027-06
AB   EP    1049165 A UPAB: 20010515
     NOVELTY - A circuit portion (2), incorporated into a well (6), includes at
     least one power transistor. A second control circuit portion (3) is
     incorporated into a second well (7). An intermediate region (4) separates
     the circuit portions. The wells and intermediate region have an opposite
     conductivity to the substrate. The intermediate region is biased at a
     potential linked to that of the first well, reducing parasitic current
     flow from the wells to substrate.
          USE - Integrated circuits for power applications.
          ADVANTAGE - Free from parasitic currents.
          DESCRIPTION OF DRAWING(S) - The drawing shows an integrated circuit
     according to the invention.
          Circuit portion 2
          Control circuit portion 3
          Intermediate region 4
          Semiconductor substrate 5
     Well 6,7
     Dwg.3/5
```

L79 ANSWER 5 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 2000-340615 [30] WPIX
DNN N2000-255762 DNC C2000-103508
TI Semiconductor component, especially a high voltage diode or thyristor, has space charge **compensation** layers associated with an opposite conductivity type lightly doped base region.
DC L03 U12
IN NAGEL, D; SITTIG, R
PA (NAGE-I) NAGEL D; (SITT-I) SITTIG R
CYC 22
PI DE 19849902 A1 20000511 (200030)* 9p H01L029-06
WO 2000026968 A1 20000511 (200031) DE H01L029-06
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: JP KR US
EP 1138083 A1 20011004 (200158) DE H01L029-06
R: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
ADT DE 19849902 A1 DE 1998-19849902 19981029; WO 2000026968 A1 WO 1999-DE3467 19991029; EP 1138083 A1 EP 1999-957954 19991029, WO 1999-DE3467 19991029
FDT EP 1138083 A1 Based on WO 200026968
PRAI **DE 1998-19849902 19981029**
IC ICM H01L029-06
ICS H01L029-744; H01L029-861; H01L029-866; H01L031-105; H01L031-111
AB DE 19849902 A UPAB: 20000624
NOVELTY - Semiconductor component has space charge **compensation** layers (6, 7) associated with an opposite conductivity type (n) lightly doped base region (3).

DETAILED DESCRIPTION - A semiconductor component has a laterally extending lightly doped first conductivity type (n) base region (3), with two lateral connection regions (1, 2) for connection to electrical contacts, and opposite second conductivity type (p) **compensation** layers (6, 7), which extend laterally within or outside the base region and have a lateral length greater than their vertical thicknesses. Preferred Features: The base material is n-conductive silicon with a dopant concentration of 1012-5 multiply 1014(especially 8 multiply 1012-1014) cm-3.

USE - Especially in power electronics, e.g. as a high voltage diode, especially a photodiode, or a thyristor, especially a light-triggered thyristor or a thyristor triode.

ADVANTAGE - The **compensation** layers provide at least partially **compensation** of space charges in the base region and allow different amounts of **compensation** in individual sections along the lateral direction, thus allowing component use at high blocking voltages in the 10-30 kV range at low production cost.

DESCRIPTION OF DRAWING(S) - The drawings show a high voltage diode with punch-through dimensioning and a diagram of the electric field in the diode.
anode region 1
cathode region 2
lightly doped base region 3
compensation layers 6, 7
Dwg.1/7

L79 ANSWER 9 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1999-612187 [53] WPIX
DNN N1999-451166
TI Semiconductor device for **compensation** element - has semiconductor zones of opposite type arranged in alternation between 2 semiconductor regions coupled to respective electrodes.
DC U11 U12
IN DEBOY, G; GRAF, H; STENGL, J; STRACK, H; WEBER, H; AHLERS, D; RUEB, M
PA (SIEI) SIEMENS AG
CYC 21
PI DE 19840032 C1 19991118 (199953)* 10p H01L029-78
WO 2000014807 A1 20000316 (200022) DE H01L029-78
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: JP KR US
EP 1114466 A1 20010711 (200140) DE H01L029-78
R: AT DE FR GB IE IT
KR 2001074945 A 20010809 (200211) H01L029-772
ADT DE 19840032 C1 DE 1998-19840032 19980902; WO 2000014807 A1 WO 1999-DE1218 19990422; EP 1114466 A1 EP 1999-929017 19990422, WO 1999-DE1218 19990422; KR 2001074945 A KR 2001-702794 20010302
FDT EP 1114466 A1 Based on WO 200014807
PRAI **DE 1998-19840032 19980902**
IC ICM H01L029-772; H01L029-78
ICS H01L021-336; H01L029-06
AB DE 19840032 C UPAB: 19991215
The semiconductor device has a semiconductor body with a pn junction, provided with alternating semiconductor zones (4,5) of opposite conductivity type extending between 2 semiconductor regions (15,16) coupled to respective electrodes.

The doping of the alternating semiconductor zones is varied between the 2 surfaces (A,B) facing the latter semiconductor regions, so that charge carriers of opposite type predominate adjacent each surface, with the electrical field having a gradient characteristic.

USE - For use as **compensation** element.

ADVANTAGE - Robust semiconductor device with defined **compensation** characteristic.
Dwg.1/8
FS EPI
FA AB; GI

L79 ANSWER 6 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 2000-339794 [29] WPIX
DNN N2000-255057
TI Power semiconductor component, such as transistor, for application as switch or converter - uses cooled technological equipment which utilises superconductivity for maintaining operating temperature of semiconductor.
DC U11 U12 X12
IN DEBOY, G; SCHLOEGL, A; SCHULZE, H
PA (SIEI) SIEMENS AG
CYC 21
PI WO 2000024061 A1 20000427 (200029)* DE 24p H01L029-78
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: JP KR US
ADT WO 2000024061 A1 WO 1999-DE3318 19991015
PRAI **DE 1998-19847820 19981016**
IC ICM H01L029-78
ICS H01L023-44; H01L029-08; H01L029-808
ICA H02J015-00
AB WO 200024061 A UPAB: 20000617
Power semiconductor component includes an additional zone between a second zone (6), of a second conductivity type, opposite to that of a first zone (7), and a third zone (1) of the first conductivity zone. At least two zones (4;5) of different conductivity type are contained in the additional zone and border one another in a direction transverse to the direction of current flow.

The component can be held to a temperature of less than 250 Kelvin during operation.

USE - As **compensation** component, based on mutual **compensation** of charge in n-doped and p-doped zones in drift region, and include MOSFET, diode, thyristor and GTO devices.

ADVANTAGE - Has significantly reduced static and dynamic power dissipation. Power switch suitable for low temperature applications.
Dwg.1/6
FS EPI
FA AB; GI

L79 ANSWER 7 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 2000-283719 [24] WPIX
DNN N2000-213492
TI Semiconductor component manufacturing method esp. for **compensation** components, such as transistors - involves forming intermediate interlocking zones of first and second conductivity type by doping out of **trenches** with subsequent filling.
DC U12
IN DEBOY, G; FRIZA, W; HAEBERLEN, O; RUEB, M; STRACK, H; HABERLEN, O; RUB, M
PA (SIEI) SIEMENS AG; (INFN) INFINEON TECHNOLOGIES AG; (DEBO-I) DEBOY G; (FRIZ-I) FRIZA W; (HABE-I) HABERLEN O; (RUBM-I) RUB M; (STRA-I) STRACK H
CYC 22
PI WO 2000017937 A2 20000330 (200024)* DE 45p H01L029-78
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: JP KR US
DE 19843959 A1 20000406 (200024) H01L021-334
EP 1110244 A1 20010627 (200137) DE H01L029-78
R: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
US 2001053568 A1 20011220 (200206) H01L021-332
KR 2001075354 A 20010809 (200211) H01L029-78
AB WO 200017937 A UPAB: 20020215
The method involves providing for a semiconductor component comprising a semiconductor body having a blocking pn-junction, a first zone (7) of a first conductivity type joined to a first electrode (10) and adjoining a zone (6) which forms the blocking pn-junction and which has a second conductivity type opposite to that of the first; a second zone (1) of the first conductivity type is connected to a second electrode. The **side** of zone (6) facing the second zone (10 forms a first surface (A), and in the region between the first (A) and second (B) surfaces are interlocking zones (4,5) of first and second conductivity types.

The zones (4) and (5) are formed by doping out of **trenches** (11,14) with subsequent filling, so that in the regions (I) near the first surface (A) **charge carriers** of the second conductivity type predominate and in regions (III) near the second surface (B) **charge carriers** of the first conductivity type predominate.

USE - For n-**channel** and p-**channel** MOSFETs, diodes, thyristors, GTOs etc.

ADVANTAGE - Enables manufacture of first and second conductivity type zones with required variable doping.
3,4a,16/16

L79 ANSWER 27 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1994-028038 [04] WPIX
CR 1994-058801 [08]; 1996-425076 [42]; 1996-442109 [44]; 1999-356853 [30]; 2000-022089 [02]
DNN N1994-021756
TI Field effect transistor for power applications - has additional lightly **doped** upper **epitaxial** layer reducing electric field at bottom of gate electrode **trench**..
DC U12
IN CHANG, M F; HSHIEH, F; KWAN, S; OWYANG, K
PA (SILI-N) SILICONIX INC
CYC 6
PI

EP 580452	A1	19940126 (199404)*	EN	8p	H01L029-60
R: DE IT NL					
JP 06224437	A	19940812 (199437)		7p	H01L029-784
US 5532179	A	19960702 (199632)		7p	H01L021-335
EP 580452	B1	19970409 (199719)	EN	10p	H01L029-423
R: DE IT NL					
DE 69309565	E	19970515 (199725)			H01L029-423
KR 305978	B	20011215 (200249)			H01L029-78

AB EP 580452 A UPAB: 20020802
The field effect transistor has its gate electrode located in a **trench** (54). The transistor includes a lightly **doped** **epitaxial** layer (46) overlying the usual **epitaxial** layer (42). The **trench** penetrates only part way through the lightly **doped** upper **epitaxial** layer.

The lightly **doped** upper **epitaxial** layer reduces the electric field at the bottom of the **trench,** thus protecting the gate oxide from breakdown during high voltage operation. Pref. the upper portion of the lightly **doped** upper **epitaxial** layer has little adverse effect on the transistor's on resistance.

ADVANTAGE - Achieves higher breakdown voltage without excessively increasing source-drain ON resistance without additional masking steps.
Dwg.2/3g

ABEQ US 5532179 A UPAB: 19960819
<E8-Abstract PN=5532179>

A DMOS field effect transistor having its gate electrode located in a **trench** includes a lightly **doped** **epitaxial** layer overlying the usual **epitaxial** layer. The **trench** penetrates only part way through the upper **epitaxial** layer which is more lightly **doped** than is the underlying lower **epitaxial** layer. The lightly **doped** upper **epitaxial** layer reduces the electric field at the bottom of the **trench,** thus protecting the gate oxide from breakdown during high voltage operation. Advantageously the upper portion of the lightly **doped** upper **epitaxial** layer has little adverse effect on the transistor's on resistance.

<E3-Claims PN=5532179>

We claim:

1. A method of making a field effect transistor comprising the steps of:

providing a substrate of a first conductivity type and having a principal surface;

growing a first **epitaxial** layer of the first conductivity type on the principal surface, the first **epitaxial** layer having a **doping** level less than that of the substrate;

growing a second **epitaxial** layer of the first conductivity type on the first **epitaxial** layer, the second **epitaxial** layer having a **doping** level less than that of the first **epitaxial** layer;

forming a body **region** of a second conductivity type in the second **epitaxial** layer and extending to a principal surface

thereof, the body **region** extending at least partly into the first **epitaxial** layer;
forming a source **region** of the second conductivity type in the body **region** and extending to the principal surface thereof;
forming a **trench** extending from the principal surface of the second **epitaxial** layer through the source **region** and the body **region**, but not extending into the first **epitaxial** layer; and
filling the **trench** at least partially with a conductive gate electrode material.
2. The method of claim 1, wherein the **trench** extends to within 0.5 microns of the first **epitaxial** layer, and the level of **doping** of the second **epitaxial** layer is about 50% that of the first **epitaxial** layer.
Dwg.2/3

ABEQ EP 580452 B UPAB: 19970512
A field effect transistor comprising a substrate (40) of a first conductivity type being a drain **region**, a lower layer (42) of the first conductivity type formed on the substrate and having a **doping** level less than that of the substrate;
an upper layer (46) of the first conductivity type formed on the lower layer and having a **doping** level less than that of the lower layer, a **trench** defined in only the upper layer and extending to within a predetermined distance of the lower layer (42), the **trench** being lined with a gate oxide layer (56) and at least partially filled with a conductive gate electrode (60), a source **region** (52) of the first conductivity type formed in the upper layer (46) and extending to the upper surface of the upper layer (46) adjacent to the **sidewalls** of the **trench**; and a body **region** (50) of a second conductivity type formed in the upper layer (46) adjacent to the source **region**, characterised in that the body **region** extends downwards from the upper surface of the upper layer (46) on each **side** of the **trench** to a depth greater than that of the **trench**, and is laterally spaced from a lower most portion of the **trench** on each **side** thereof, and characterised in that the body **region** extends into at least an upper portion of the lower layer and to a depth greater than that of the lowest portion of the upper layer thereby delimiting the **sides** of the upper layer laterally.
Dwg.2/3g

FS EPI

L79 ANSWER 53 OF 64 JAPIO COPYRIGHT 2002 JPO
AN 1998-070275 JAPIO
TI DEFECT FORMATION CONTROL METHOD IN FABRICATION OF SILICON **INTEGRATED** CIRCUIT, METHOD FOR CONTROLLING QUALITY AND DEFECT FORMATION OF OXIDE, DOUBLE DIFFUSION **INTEGRATED** CIRCUIT DEVICE, AND FORMATION OF **INTEGRATED** CIRCUIT MOSFET CELL
IN YILMAZ HAMZA; HSHIEH FWU-IUAN; CHANG MIKE
PA SILICONIX INC
PI JP 10070275 A 19980310 Heisei
AI JP 1997-209312 (JP09209312 Heisei) 19970804
PRAI US 1990-631569 19901221
US 1990-631573 19901221
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1998
IC ICM H01L029-78
ICS H01L021-265; H01L021-322
AB PROBLEM TO BE SOLVED: To promote load management switching more efficiently by forming a surface adjacent composite **region** in three **regions** of second conductivity type and locating a source in a part of the composite **region** while separating from the semiconductor material of a semiconductor body on the outside of the composite **region**.
SOLUTION: An n-type lightly **doped epitaxial** silicon layer 1 has various diffusion **regions**, e.g. deep p+ **regions** 2, 3, p-body **regions** 4, 5 and n+ source **regions** 6, 7. A continuous source body electrode 12 normally extends to some surface part of the **epitaxial** layer 1. A drain electrode is provided on the rear **side** of an n+ **doped** substrate. An insulation gate structure comprising a gate oxide 16 and a polysilicon 18 is provided on the drain and respective parts of the body and the latter functions as an MOSFET **channel region**.
Basic elements of a simplified resistor circuit comprises **channel** resistors 20, 21 JFET resistors 22-24 and an epi-resistor 26.

L79 ANSWER 63 OF 64 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:637423 HCAPLUS
DN 125:290735
TI **Trench** field-effect transistor with reduced punchthrough susceptibility and low source-to-drain resistance in the ON state (RDSon)
IN Hshieh, Fwu-iuan; Chang, Mike F.
PA Siliconix Inc., USA
SO U.S., 8 pp., Cont.-in-part of U.S. Ser. No. 918,954.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L029-76
ICS H01L029-94
NCL 257342000
CC 76-3 (Electric Phenomena)
FAN.CNT 3

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE	
PI	US 5558313	A	19960924	US 1995-386895	19950210	<--
	US 5910669	A	19990608	US 1992-918954	19920724	
	JP 06104445	A2	19940415	JP 1993-210844	19930802	<--
	EP 583911	A1	19940223	EP 1993-306133	19930803	<--
	R: DE, IT, NL					
	US 5479037	A	19951226	US 1993-131114	19931001	<--
	CA 2212765	AA	19960815	CA 1996-2212765	19960207	<--
	WO 9624953	A1	19960815	WO 1996-US941	19960207	<--
	US 5981344	A	19991109	US 1996-658115	19960604	<--
	US 5770503	A	19980623	US 1997-895004	19970717	<--

AB To reduce susceptibility to punchthrough, the **channel region** of the P body **region** of a **trench** FET is formed in a layer of lightly **doped epitaxial** Si. As a result, the **channel region** has less counterdoping from the background **epitaxial** Si and has a greater net P-type **dopant** concn. Due to the higher net **dopant** concn. of the P body **region**, the depletion **regions** on either **side** of the P body **region** expand less far inward through the P body **region** at a given voltage, thereby rendering the transistor less susceptible to source-to-drain punchthrough. To maintain a low RDSon, the relatively high cond. of an accumulation **region** formed along a **sidewall** of the **trench** of the transistor when the transistor is ON is used to form a conductive path from the **channel region** to an underlying relatively highly conductive layer on which the lightly **doped epitaxial** layer is formed. This underlying relatively highly conductive layer may, e.g., be either the substrate or a more heavily **doped epitaxial** Si layer.
ST **trench** field effect transistor reduced punchthrough; source

L79 ANSWER 8 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 2000-022089 [02] WPIX
CR 1994-028038 [04]; 1994-058801 [08]; 1996-425076 [42]; 1996-442109 [44]; 1999-356853 [30]
DNN N2000-016350 DNC C2000-005286
TI **Trench** double diffused field effect transistor having reduced punch-through susceptibility.
DC L03 U11 U12
IN CHANG, M F; HSIEH, F
PA (SILI-N) SILICONIX INC
CYC 1
PI US 5981344 A 19991109 (200002)* 9p H01L021-336
ADT US 5981344 A CIP of US 1992-918954 19920724, Cont of US 1992-925336 19920804, CIP of US 1993-131114 19931001, Div ex US 1995-386895 19950210, US 1996-658115 19960604
FDT US 5981344 A CIP of US 5479037, Div ex US 5558313
PRAI **US 1995-386895 19950210; US 1992-918954 19920724 ; US 1992-925336 19920804; US 1993-131114 19931001; US 1996-658115 19960604**
IC ICM H01L021-336
AB US 5981344 A UPAB: 20020802

NOVELTY - The method comprises forming a lower layer of a first conductivity type on a substrate of a first conductivity type, wherein the lower layer has a **doping** level less than that of the substrate.

DETAILED DESCRIPTION - The method comprises forming a lower layer of a first conductivity type on a substrate of a first conductivity type, wherein the lower layer has a **doping** level less than that of the substrate. An upper layer of the first conductivity type and having a **doping** level less than that of the lower layer is formed to entirely overlay the lower layer, and a **trench** is defined in the upper and lower layers extending to within a predetermined distance of the substrate. The **trench** is filled with a conductive gate electrode, and a source **region** of the first conductivity type is formed in the upper layer adjacent its principal surface and adjacent the **sidewalls** of the **trench**. A body **region** of a second conductivity type is formed extending from the principal surface of the upper layer down to and into an upper portion of the lower layer, and spaced apart from a lower portion of the **trench**, wherein 2 spaced apart portions of the body **region** lying respectively on 2 **sides** of the **trench** define a lateral extent of the upper layer.

USE - A method of forming a **trench** double diffused field effect transistor.

ADVANTAGE - The power field effect transistor has both low source-to-drain resistance as well as the ability to withstand high source-to-drain voltages without suffering punch-through problems.

DESCRIPTION OF DRAWING(S) - The drawing shows a simplified cross-section of a **trench** double diffused field effect transistor.

Lightly **doped** N- type **epitaxial** layer 201
Heavily **doped** N+ type substrate layer 203
P body **region** 204
Gate **region** 209A
Dwg.6/7

FS CPI EPI

L79 ANSWER 11 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1998-481456 [41] WPIX
DNN N1998-375592
TI Insulated gate bipolar transistor structure - includes base zone embedded in screening zone of first conductivity and having higher doping concentration than surrounding inner zone.
DC U12
IN HIRLER, F; PFIRSCH, F; WERNER, W
PA (SIEI) SIEMENS AG; (SIEI) INFINEON TECHNOLOGIES AG
CYC 20
PI WO 9838681 A1 19980903 (199841)* DE 18p H01L029-739
RW: AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: JP KR US
DE 19707513 A1 19980924 (199844) H01L029-78
EP 913000 A1 19990506 (199922) DE H01L029-739
R: DE FR GB IE IT
JP 2000509916 W 20000802 (200042) 14p H01L029-78
US 6147381 A 20001114 (200060) H01L029-72
KR 2000064987 A 20001106 (200128) H01L029-739

AB WO 9838681 A UPAB: 19981014

The IGBT structure includes a semiconductor (1) with an inner zone (2) of first conductivity type bordering on the upper face (3) of the semiconductor. An anode zone (5) of second conductivity type, and at least one base zone (6) of second conductivity are embedded into the upper face (3) of the semiconductor.

At least one emitter zone (7) of first conductivity type is embedded into the base zone (6) and it has an emitter electrode (8) connected to it. Also provided is a collector electrode (9) on the underside and a gate electrode (10) on the upper surface. The base zone (6) is embedded in a screening zone (13) of first conductivity type which has a higher doping concentration than the surrounding inner zone (2) in the region of which is provided at least one floating, unconnected region (15) of high conductivity of second conductivity type the lower edge (16) of which lies deeper in the inner zone (2) than the lower edge (14) of the screening zone (13).

ADVANTAGE - Uses planar technology for IGBT yet achieves parameter of IGBT with **trench** technology e.g. V-shaped and U-shaped **groove** without resorting to complicated non-planar **trench** structure technology during manufacture. Reduced forward current as minority **carrier** density on cathode **side** is increased.
Breakdown voltage is not reduced as inner zone no longer acts as minority **carrier** sink.

L79 ANSWER 12 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1997-274103 [25] WPIX
DNN N1997-227021
TI MOS technology power transistor e.g. MOSFET or IGBT - has lightly doped region within semiconductor material layer e.g. epilayer and beneath transistor element body regions, to fix transistor breakdown voltage.
DC U11 U12
IN FERLA, G; FRISINA, F; RINAUDO, S
PA (CONS-N) CONSORZIO RICERCA SULLA MICROELETTRONICA; (SGSA) SGS THOMSON MICROELTRN SRL; (SGSA) STMICROELECTRONICS SRL
CYC 6

PI	EP 772244	A1 19970507	(199725)*	EN	9p	H01L029-78
	R: DE FR GB IT					
	JP 09232567	A 19970905	(199746)		9p	H01L029-78
	US 5900662	A 19990504	(199925)			H01L029-62
	EP 772244	B1 20000322	(200019)	EN		H01L029-78
	R: DE FR GB IT					
	DE 69515876	E 20000427	(200027)			H01L029-78
	US 6228719	B1 20010508	(200128)			H01L021-336

AB EP 772244 A UPAB: 19970619
The MOS technology power device includes functional elements e.g. polygonal cells or stripes, each having a body region formed in an opposite conductivity type semiconductor layer. There is a lightly doped region beneath each body region, of the same conductivity type as the semiconductor layer and having a higher resistivity value than the resistivity of the layer. Pref. the resistivity of the lightly doped regions determines the breakdown voltage of the MOS power transistor.

Pref. the lightly doped regions contain dopant which partially **compensate** the concentration of dopant in the semiconductor layer, and have a high diffusivity in the layer. The transistor may be formed over a heavily doped semiconductor substrate, with the lightly doped region extending to the substrate. The substrate may be n-type or p-type. The transistor elements may be doped p-type or n-type.

USE - E.g. low voltage, 30-200 V, devices.

ADVANTAGE - Lower resistivity common drain layer for lower output resistance; less distance between transistor elements and reduced gate-drain capacitance.
Dwg.0/8

L79 ANSWER 24 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1995-221795 [29] WPIX
CR 1993-054325 [07]; 2002-473142 [51]
DNN N1995-173865
TI Insulated gate type semiconductor element e.g. MOS controlled thyristor for high power use - forms P type base layer with **trench** on N type base layer where gate electrode embedded with insulating film N type source formed outside.
DC U12
IN INOUE, T; KITAGAWA, M; NAKAGAWA, A; OMURA, I; YASUHARA, N
PA (TOKE) TOSHIBA KK
CYC 2

PI						
	JP 07135309	A	19950523	(199529)*	25p	H01L029-78
	US 5448083	A	19950905	(199541)	116p	H01L021-36
	US 5585651	A	19961217	(199705)	117p	H01L029-74
	US 5689121	A	19971118	(199801)	114p	H01L029-74
	US 5838026	A	19981117	(199902)		H01L021-36

AB JP 07135309 A UPAB: 20020815
The insulated gate type semiconductor element consisting of a P type emitter layer (1) on which an N type high resistance base layer (3) is formed. A P type base layer (4) is formed over the N type high resistance base layer. A **trench** slot is formed in the N type high resistance base layer from the surface of the P type base layer. The **trench** slot is covered by a gate insulating film (6) between which the gate electrode (7) is embedded.

An N type source layer is formed in the surface of the P type base layer contacting the outer **side** surface of the **trench** slot. This constitutes first MOST. A hole is discharged out of the element by a second MOST (10) connected to the first one.

ADVANTAGE - Improves turn ON/OFF characteristics.
Dwg.1/42

ABEQ US 5448083 A UPAB: 19951019
An insulated-gate semiconductor device includes a P type emitter layer, an N- high-resistive base layer formed on the P type emitter layer, and a P type base layer contacting the N- high-resistive base layer. A number of **trenches** are formed having a depth to reach into the N- high-resistive base layer from the P type base layer. A gate electrode covered with a gate insulation film is buried in each **trench**.

An N type source layer to be connected to a cathode electrode is formed in the surface of the P type base layer in a **channel** region between some **trenches**, thereby-forming an N **channel** MOS transistor for turn-on operation. A P **channel** MOS transistor connected to the P base layer is formed in a **channel** region between other **trenches** so as to discharge the holes outside the device upon turn-off operation.

ADVANTAGE - Device has low on-resistance and high current cut-off ability to attain enhanced withstanding voltage characteristic.
Dwg.2/147

ABEQ US 5585651 A UPAB: 19970129
A semiconductor device comprising:

a first semiconductor layer serving as a base layer;

a second semiconductor layer connected to said base layer for allowing first type **charge carriers** to be injected into said base layer;

a third semiconductor layer connected to said base layer for allowing second type **charge carriers** to be injected into said base layer to cause a conductivity modulation to occur therein;

a fourth semiconductor layer connected to said base layer for allowing said first type **charge carriers** contained in said base layer to move externally out of said base layer, said fourth semiconductor layer comprising spaced-apart first and second portions;

a plurality of **trenches** formed in said base layer, each

having a depth, a width and a length and being surrounded by an insulating **wall,** said **trenches** being spaced apart in a direction along said width such that a plurality of gap regions including first, second and **dummy** gap regions are formed therebetween, said **dummy** gap region being arranged between said first and second gap regions, said first and second gap regions defining narrow current paths respectively connecting said first and second portion of said fourth semiconductor layer to said base layer for allowing said first type **charge carriers** to flow therein;

a MOS **channel** for selectively connecting said base layer and said third semiconductor layer in order to thereby turn on and turn off said device;

a gate electrode facing said MOS **channel;**

a first main electrode connected to said second semiconductor layer;

a second main electrode connected to said third semiconductor layer and said first and second portions of said fourth semiconductor layer; and

an insulating cover layer directly covering said **dummy** gap region.

Dwg.2/147

ABEQ US 5689121 A UPAB: 19980107

The insulated gate type semiconductor element consisting of a P type emitter layer (1) on which an N type high resistance base layer (3) is formed. A P type base layer (4) is formed over the N type high resistance base layer. A **trench** slot is formed in the N type high resistance base layer from the surface of the P type base layer. The **trench** slot is covered by a gate insulating film (6) between which the gate electrode (7) is embedded.

An N type source layer is formed in the surface of the P type base layer contacting the outer **side** surface of the **trench** slot. This constitutes first MOST. A hole is discharged out of the element by a second MOST (10) connected to the first one.

ADVANTAGE - Improves turn ON/OFF characteristics.

Dwg.2/147

FS EPI

L79 ANSWER 13 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1997-124939 [12] WPIX
DNN N1997-103189
TI Power semiconductor device e.g. IGBT - in which gate electrode is formed inside **trench** through gate insulating film where **side** area between **trench** which contact gate electrode is detected along predetermined surface.
DC U12
IN INOUE, T; OHASHI, H; OMURA, I
PA (TOKE) TOSHIBA KK
CYC 2

PI	JP 09008301	A	19970110 (199712)*	13p	H01L029-78
	US 5714775	A	19980203 (199812)	27p	H01L029-74

ADT JP 09008301 A JP 1996-57641 19960314; US 5714775 A US 1996-633688 19960419
PRAI **JP 1995-95500 19950420**
IC ICM H01L029-74; H01L029-78
ICS H01L031-111
AB JP 09008301 A UPAB: 19970320
The device has a P type emitter layer (2) which is formed on the back **side** of an N type base layer (1). The P type emitter layer has low insulation characteristics whereas N base layer has high insulating characteristics. A P type base layer (3) is formed in the surface of the N type base layer. Multiple **trenches** (17) are formed by penetrating both the P type and N type base layers.

An upper N type emitter layer (4) of low insulating nature is formed in the surface of the P type layer which touches the **trench**. Then, a gate electrode (5) is formed inside the **trench**, through gate insulating film. The **side** face area between **trenches** which touches gate electrode is formed along predetermined surface (100).

ADVANTAGE - Increases amount of **carrier** stored in base layer. Reduces conducting loss.
Dwg.1/25
ABEQ US 5714775 A UPAB: 19980323
The device has a P type emitter layer (2) which is formed on the back **side** of an N type base layer (1). The P type emitter layer has low insulation characteristics whereas N base layer has high insulating characteristics. A P type base layer (3) is formed in the surface of the N type base layer. Multiple **trenches** (17) are formed by penetrating both the P type and N type base layers.

An upper N type emitter layer (4) of low insulating nature is formed in the surface of the P type layer which touches the **trench**. Then, a gate electrode (5) is formed inside the **trench**, through gate insulating film. The **side** face area between **trenches** which touches gate electrode is formed along predetermined surface (100).

ADVANTAGE - Increases amount of **carrier** stored in base layer. Reduces conducting loss.
Dwg.1/28
FS EPI

L79 ANSWER 15 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1997-023516 [03] WPIX
CR 1997-035939 [04]; 1997-052679 [05]
DNN N1997-019513
TI Integrated circuit with quasi-vertical DMOS device and matched pilot transistor - includes isolated pilot transistor with symmetrical gate and drain, corresp. to power device array symmetry, and has pilot drain diffusion fabricated to **compensate** pilot source current.
DC U12 U13
IN PEARCE, L G
PA (HARO) HARRIS CORP
CYC 6
PI EP 747969 A1 19961211 (199703)* EN 9p H01L029-78
R: DE FR GB IT SE
US 5684305 A 19971104 (199750) 7p H01L029-78
EP 747969 B1 19990526 (199925) EN H01L029-78
R: DE FR GB IT SE
DE 69602555 E 19990701 (199932) H01L029-78
ADT EP 747969 A1 EP 1996-400695 19960329; US 5684305 A US 1995-483692 19950607; EP 747969 B1 EP 1996-400695 19960329; DE 69602555 E DE 1996-602555 19960329, EP 1996-400695 19960329
FDT DE 69602555 E Based on EP 747969
PRAI **US 1995-483692 19950607**
REP 1.Jnl.Ref; DE 4209148; EP 557253; JP 05267675; US 5256893
IC ICM H01L029-78
ICS H01L027-02
AB EP 747969 A UPAB: 19970205
The IC includes a pilot transistor matched to a quasi-vertical DMOS transistor. The integrated power device is a fully isolated power DMOS device. The pilot transistor includes body and source regions located in an epilayer of the IC, and respectively the same as the quasi-vertical DMOS body and source regions. The pilot transistor has a gate electrically isolated from the epilayer and partly covering some of the epilayer surface between the pilot body and source regions. The pilot transistor also includes a buried layer and a drain region, which have resistances corresponding to respective DMOS buried layer and drain resistances.

Pref. the pilot gate is shaped corresp. to the symmetry of the DMOS gate around a DMOS source cell in the DMOS array, and the pilot drain region is similarly shaped, formed in the IC substrate. The pilot is isolated from the DMOS power device. The pilot drain resistance may be greater than the DMOS drain resistance.

ADVANTAGE - Pilot accurately matches DMOS performance.
Dwg.4/4
ABEQ US 5684305 A UPAB: 19971217
In an integrated circuit formed in a semiconductor substrate and comprising a QVDMOS power device having a symmetrical source array with each source disposed in a body region, a buried layer beneath the source array, a drift region disposed between the body and the buried layer, a channel region, and a drain region in contact with the buried layer, wherein the total resistance of the QVDMOS power device comprises combined resistances of the channel region, the drift region and the buried layer an improvement comprising:

a pilot transistor, electrically isolated from the QVDMOS power device and having a pilot gate, a pilot body, a pilot source, a pilot channel, a pilot drift region and a pilot buried layer region wherein the total pilot resistance comprises the combination of the pilot channel, pilot drift and pilot buried layer resistances and

a **compensating** resistance located between the pilot buried layer and the pilot drain, said **compensating** resistance having a magnitude sufficient to raise the total pilot drift resistance of the pilot transistor to the same proportion of the total pilot resistance as the proportion of the QVDMOS drift resistance to the total QVDMOS

transistor resistance.
Dwg.4/4
FS EPI

L79 ANSWER 18 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1996-309809 [31] WPIX
DNN N1996-260261
TI Current limiting circuit with JFET for input protection of load e.g. gas discharge lamps - has JFET formed with opposite conductivity buried regions within transistor substrate operating as floating gate electrode, and separating **channel** regions between source-drain electrodes on opposite surfaces.
DC U12 U13
IN LUDIKHUIZE, A W
PA (PHIG) PHILIPS ELECTRONICS NV; (PHIG) KONINK PHILIPS ELECTRONICS NV; (PHIG) PHILIPS NORDEN AB; (PHIG) US PHILIPS CORP
CYC 19
PI WO 9619831 A2 19960627 (199631)* EN 15p H01L023-58
RW: AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
W: CN JP
WO 9619831 A3 19960829 (199643) H01L023-58
EP 745273 A1 19961204 (199702) EN 15p H01L023-62
R: DE FR GB IT NL
JP 09509789 W 19970930 (199749) 21p H01L021-337
US 5747841 A 19980505 (199825) 9p H01L029-772
EP 745273 B1 19981028 (199847) EN H01L023-62
R: DE FR GB IT NL
DE 69505646 E 19981203 (199903) H01L023-62
CN 1145138 A 19970312 (200103) H01L023-62
AB WO 9619831 A UPAB: 19961004
The circuit supplies an operating voltage to a load and includes a semiconductor element having two main electrodes connected so that the input current flows through the electrodes. The circuit limits an input current which passes through input **terminals** during operation, with the **terminals** connected to the supply voltage poles. The semiconductor element is pref. a JFET, and has the two current-carrying electrodes at opposite **sides**. Each electrode is formed by a high doping concn. region at the respective surface, with the adjoining substrate having a lower doping concn. between the electrode regions.

The substrate doping and thickness is chosen so that current saturation occurs when the voltage across the electrodes rises above a set voltage e.g. due to mobile **charge carrier** velocity saturation. The JFET pref. includes buried regions of opposite conductivity to the electrode regions, located within the substrate to form an electrically floating gate and define interspersed transistor **channel** regions. The buried regions may be shaped as regular hexagons in a honeycomb pattern. The current flow within the JFET is transverse to the transistor surfaces, and saturates when the transistor drain-source voltage exceeds the pinch-off voltage.

USE/ADVANTAGE - Lamp ballast circuit, with several discharge lamps on common switch; protects against high peak currents when mains supply is at max. during switch-on. No control circuit required; symmetrical construction, so that element can be placed both in front of and behind rectifier bridge.
Dwg.2/8

L79 ANSWER 19 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1996-177786 [18] WPIX
DNN N1996-149472 DNC C1996-056061
TI Semiconductor device in motor drive circuit for voltage **compensation** - has third electrode set up at bottom surface of semiconductor substrate..
DC L03 U11 U12
PA (ROHL) ROHM CO LTD
CYC 1
PI JP 08055999 A 19960227 (199618)* 5p H01L029-861
ADT JP 08055999 A JP 1994-188289 19940810
PRAI **JP 1994-188289 19940810**
IC ICM H01L029-861
ICS H01L021-761
AB JP 08055999 A UPAB: 19960503
The semiconductor device consists of an n-type epitaxial growth layer (2) set up on a p-type semiconductor substrate (1). A p-type domain (4) is provided in the epitaxial growth layer and an n-type domain (5) is set up within that. A first diode (3a) is equipped at a pn junction (3) formed between the substrate and epitaxial layer.

A second diode (6a) is formed at a second pn junction (6). A first electrode (7) is connected to both regions of the epitaxial growth layer and the p-type domain. A second electrode (8) is connected to an n-type domain and a third electrode (9) is set up at the bottom surface of the substrate.

USE/ADVANTAGE - In e.g. a full wave rectifier mfr. is enabled at low cost with a reduced number of processes by using same chip area in same time. Improves breakdown voltage.
Dwg.1/8
FS CPI EPI

L79 ANSWER 20 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1996-039617 [04] WPIX
CR 1994-263281 [32]
DNN N1996-033376 DNC C1996-013328
TI Process for mfr. of radiation-resistant power MOSFET - forms gate oxide near end of process to avoid thermal cycling and uses arsenic dopant.
DC L03 U12 W06
IN MERRILL, P; SPRING, K A
PA (INRC) INT RECTIFIER CORP
CYC 1
PI US 5475252 A 19951212 (199604)* 9p H01L029-78
ADT US 5475252 A Cont of US 1987-1629 19870108, US 1994-288585 19940810
FDT US 5475252 A Cont of US 5338693
PRAI **US 1987-1629 19870108; US 1994-288585 19940810**
IC ICM H01L029-78
ICS H01L023-48
AB US 5475252 A UPAB: 19960129

A MOS-gated semiconductor device having short-circuit current-limiting ballasting comprises a single crystal Si die having a doped upper surface and many laterally spaced, oppositely doped channel regions (44) and a source for each channel (50) of less depth than the channel. A gate electrode (61) on, and insulated from (60), the channel, can invert the channel on voltage application, a metallic electrode (90) connects to each source, which has a relatively high resistance region in-series with the metal electrode, channel and body path, and the metallic electrode forms a Schottky barrier of increased resistance to the relatively high resistance portions to act as parallel ballasting resistor and limit short-circuit current.

USE - In the mfr. of radiation-resistant power MOSFET's for, e.g. **free** space uses and in nuclear radiation environments.

ADVANTAGE - The MOSFET has a high voltage rating, is not susceptible to gate-to-source threshold voltages changes due to ionising radiation, and the ON resistance is not degraded by high neutron fluxes.

Dwg.13/13

L79 ANSWER 21 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1995-285002 [38] WPIX
CR 2002-218481 [28]
DNN N1995-217007
TI Insulated gate semiconductor device with **trench** gate e.g. power MOS transistor or IGBT - includes ladder-like emitter layer in semiconductor substrate upper surface, between adjacent stripe **trenches** having buried gate electrodes and forming continuous **channel** region along **trench**.
DC U11 U12
IN HARADA, M; MINATO, T; NISHIHARA, H; TAKAHASHI, H
PA (MITQ) MITSUBISHI DENKI KK; (MITQ) MITSUBISHI ELECTRIC CORP
CYC 6

PI	EP 668616	A2	19950823	(199538)*	EN	69p	H01L029-08
	R: DE FR GB						
	JP 07235672	A	19950905	(199544)		35p	H01L029-78
	EP 668616	A3	19951011	(199616)			H01L029-08
	US 6107650	A	20000822	(200042)			H01L029-749
	KR 199273	B1	19990615	(200059)			H01L029-78
	EP 668616	B1	20011017	(200169)	EN		H01L029-08
	R: DE FR GB						
	US 6323508	B1	20011127	(200175)			H01L029-749
	DE 69523192	E	20011122	(200201)			H01L029-08
	US 6331466	B1	20011218	(200205)			H01L021-336

AB EP 668616 A UPAB: 20020502
The semiconductor device includes a substrate with an N+ buffer layer. The substrate is a P+ collector. Base and emitter layers are diffused into an N- layer on the buffer layer. The substrate has several **trenches** formed from its upper surface down through the base and emitter layers, in stripes and perpendicular to the comb-like gate interconnection.

Gate insulating film covers an inner **wall** of the **trench** and a polysilicon gate electrode is buried in the **trench**.

ADVANTAGE - Enhanced **integration** due to easy miniaturisation. Simple processing. Increased breakdown tolerance due to structure. Decreased ON voltage due to miniaturisation. Ensures reliable emitter electrode contact to emitter layer
Dwg.1/45
FS EPI

L79 ANSWER 22 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1995-265119 [35] WPIX
DNN N1995-203999
TI Power factor correction pre-**compensation** circuit - switches power transistor across junction of boost inductor and rectifier according to variable duty cycle.
DC U24
IN BALAKRISHNAN, B; LEMAN, B R
PA (POWE-N) POWER INTEGRATIONS INC
CYC 8
PI EP 665630 A2 19950802 (199535)* EN 10p H02M003-156
R: DE FR GB IT NL SE
US 5461303 A 19951024 (199548) 9p G05F001-652
JP 07303331 A 19951114 (199603) 6p H02J003-18
EP 665630 A3 19950927 (199615) H02M003-156
EP 665630 B1 20020508 (200231) EN H02M003-156
R: DE FR GB IT NL SE
DE 69526601 E 20020613 (200246) H02M003-156
ADT EP 665630 A2 EP 1995-101110 19950127; US 5461303 A US 1994-189422 19940131; JP 07303331 A JP 1995-13033 19950130; EP 665630 A3 EP 1995-101110 19950127; EP 665630 B1 EP 1995-101110 19950127; DE 69526601 E DE 1995-626601 19950127, EP 1995-101110 19950127
FDT DE 69526601 E Based on EP 665630
PRAI **US 1994-189422 19940131**
REP No-SR.Pub; 1.Jnl.Ref; US 5008599; WO 8501400; WO 8905057
IC ICM G05F001-652; H02J003-18; H02M003-156
ICS H02M003-155; H02M007-217
AB EP 665630 A UPAB: 19950905
The circuit (10) comprises a bridge rectifier (12), a boost inductor (14), a boost rectifier (16), an output capacitor (18), a three terminal pulse width modulation (PWM) device (20), a voltage feedback circuit (22), a capacitor (24), a resistor (26), a capacitor (28) and a pre-**compensation** resistor (30). The PWM device has a power transistor that is duty cycle controlled according to the current driven into its ''C'' terminal.

The pre-**compensation** resistor delivers a current into the ''C'' terminal which is proportional to the instantaneous value of the rectified AC input voltage. The capacitors with the voltage feedback circuit provide filtering. The current through the first resistor varies the average duty cycle of the PWM device over many AC input cycles.

ADVANTAGE - Provides simple power factor correction without monitoring load and switching currents.
Dwg.1/5
ABEQ US 5461303 A UPAB: 19951204
A power factor correction circuit for connection to an alternating current power line source, comprising: a rectifier having an input connection for alternating current (AC) power with a first frequency and a full-wave rectified voltage output with a common reference connection; a boost inductor connected to said output of the rectifier; a boost rectifier connected to the boost inductor and for providing a direct current output voltage; a pulse-width modulated (PWM) device with a switch connected between said common reference connection and a junction of the boost inductor and the boost rectifier and providing for continuously variable duty-cycle on-off control of said switch at a second frequency that is fixed and substantially higher than said first frequency according to a control signal to an input; and a recompensation resistor connected between said full-wave rectified voltage output of the rectifier and said control signal input of the PWM device, and providing for linear duty-cycle variations of the PWM device that are in part affected by the instantaneous signal magnitude of said full-wave rectified output of the rectifier, wherein the average duty cycle of PWM device is constant over many cycles of said first frequency and an average filtered value of a

current flowing in said boost inductor is sinusoidal.
Dwg.1/5
FS EPI
FA AB; GI

L51 ANSWER 6 OF 203 WPIX (C) 2002 THOMSON DERWENT
AN 2000-499389 [44] WPIX
DNN N2000-370138 DNC C2000-149941
TI Formation of extended drain of high voltage field effect transistor (HVFET) having low on-state resistance.
DC L03 U11 U12
IN AJIT, J S; DISNEY, D R; RUMENNIK, V
PA (POWE-N) POWER INTEGRATIONS INC
CYC 91

PI	WO 2000046851	A1	20000810	(200044)*	EN	45p	H01L021-425
	AU 2000029770	A	20000825	(200059)			H01L021-425
	US 6168983	B1	20010102	(200103)			H01L021-337
	EP 1163697	A1	20011219	(200206)	EN		H01L021-425

PRAI **US 1999-245029 19990205**; US 1996-744182 19961105
IC ICM H01L021-337; H01L021-425
ICS H01L021-265; H01L021-8238; H01L027-02; H01L027-085; H01L029-06; H01L029-76; H01L029-78; H01L029-80; H01L029-808; H01L029-88; H01L029-94
AB WO 200046851 A UPAB: 20000913
NOVELTY - The method comprises

(a) forming a well region (17) of a first conductivity type in a substrate of a second conductivity type, the well region having a laterally extended portion (23),

(b) implanting a dopant of the second conductivity type into the laterally extended portion of the well region to form a buried region (18), and

(c) forming a drain diffusion region (19) of the first conductivity type in the well.

DETAILED DESCRIPTION - Preferred features - The buried region is disposed beneath a surface of the substrate. Step (a) comprises implanting a dopant of the first conductivity type into the substrate, and diffusing the dopant into the substrate. The first conductivity type is n-type and the second conductivity type is p-type. The drain diffusion region is spaced-apart from the buried region. The buried region is sandwiched within the well region such that dual junction FET conduction channels are formed above and below the buried region.

USE - For the manufacture of HVFET structures that include an insulated gate FET in series with a junction FET.

ADVANTAGE - A minimal number of processing steps are required to form the parallel JFET conduction channels which provide the HVFET with a low on-state resistance.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section of the HVFET.

N-well region 17
Buried region 18
Drain diffusion region 19
Lateral boundary 21
Laterally extended drain portion 23

Dwg.1/14
FS CPI EPI

L51 ANSWER 7 OF 203 WPIX (C) 2002 THOMSON DERWENT
AN 2000-498080 [44] WPIX
DNN N2000-369112
TI Lateral power MOSFET, has source electrode coupled to source region so that width of source electrode arranged near contact-free region is greater than that of source electrode near two contact regions.
DC U12
IN DISNEY, D R; DJENGUERIAN, A B
PA (POWE-N) POWER INTEGRATIONS INC
CYC 1
PI US 6084277 A 20000704 (200044)* 19p H01L031-113
ADT US 6084277 A US 1999-253319 19990218
PRAI **US 1999-253319 19990218**
IC ICM H01L031-113
ICS H01L031-119
AB US 6084277 A UPAB: 20001006

NOVELTY - A source region and a drain region are separated by a channel region (507). A source electrode (503) is coupled to the source region so that width of the source electrode near the contact region is greater than that of the source electrode near the two contact region and the overlap of the gate structure by the source electrode is greater in the contact-free region than that in the two contact regions.

DETAILED DESCRIPTION - The gate structure (513) arranged over the channel region has two contact regions (545,547) that are separated by a contact-free region. A gate electrode (509) is coupled to the gate structure in the two contact regions through the two contacts (533,535). A field plate is arranged over the channel region is extended towards the drain region the resistance between the gate electrode and the two contact regions is less than that between the gate electrode and the contact-free region. The sheet resistance of the gate structure is less than that of the gate electrode.

USE - Lateral power MOSFET used for high voltage applications.

ADVANTAGE - Enhances peak current level. Enables to achieve desired resistance for gate structure.

DESCRIPTION OF DRAWING(S) - The figure shows a side view of MOSFET.

Source electrode 503
Channel region 507
Gate electrode 509
Gate structure 513
Gate electrode contacts 533,535
Contact regions 545,547

Dwg.5A/8
FS EPI

L79 ANSWER 44 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1987-186658 [27] WPIX
CR 1991-051092 [07]; 1993-010507 [02]
DNN N1987-139515 DNC C1987-077733
TI Lateral insulated gate transistor - with anode electrode positioned for fast switching.
DC L03 U12
IN COLAK, S; RUMENNIK, V
PA (PHIG) PHILIPS GLOEILAMPENFAB NV
CYC 6
PI EP 228107 A 19870708 (198727)* EN 8p
R: DE FR GB NL
JP 62131580 A 19870613 (198729)
CA 1252225 A 19890404 (198918)
EP 228107 B1 19940622 (199424) EN 9p H01L029-72
R: DE FR GB NL
DE 3689931 G 19940728 (199429) H01L029-72
ADT EP 228107 A EP 1986-202083 19861124; JP 62131580 A JP 1986-278893 19861125; EP 228107 B1 EP 1986-202083 19861124; DE 3689931 G DE 1986-3689931 19861124, EP 1986-202083 19861124
FDT DE 3689931 G Based on EP 228107
PRAI **US 1985-802781 19851127**
REP 3.Jnl.Ref; A3...8835; DE 3011484; EP 111803; No-SR.Pub; US 4300150; 1.Jnl.Ref
IC H01L027-06; H01L029-72
ICM H01L029-72
ICS H01L027-06; H01L029-08; H01L029-10; H01L029-36; H01L029-52
AB EP 228107 A UPAB: 19930922
In a lateral insulated gate transistor, the anode electrode is situated in the **epitaxial** layer on the substrate and is coupled to the drain **region**.

The anode electrode may directly contact adjacent surface-adjoining drain and anode **regions** which are **side** by **side** and in direct contact with each other. Alternatively the drain and anode **regions** are spaced and the anode **region** is provided in a highly **doped** surface-adjoining **region** of the same conductivity type as the **epitaxial** layer. In this second case, the anode electrode is directly connected to the anode **region** and is coupled to the drain **region** through a resistive element.

ADVANTAGE - The device retains high current handling capability, low 'on' resistance, high breakdown voltage and process compatibility with bipolar and MOS control circuits, while having fast switching characteristics.
ABEQ EP 228107 B UPAB: 19940803
A semiconductor device with a lateral insulated gate field effect transistor having a semiconductor substrate of a first conductivity type, an **epitaxial** surface layer of a second conductivity type opposite to that of the first on a first major surface of said substrate, a surface adjoining **channel region** of said first conductivity type in said **epitaxial** layer and forming a pn-junction therewith, a surface adjoining source **region** of said second conductivity type in said **channel region**, a surface adjoining drain **region** of said second conductivity type in said **epitaxial** layer and spaced apart from said **channel region** by a drift **region**, an insulating layer on said **epitaxial** surface layer and covering at least that portion of said **channel region** located between said source **region** and said drain **region**, a gate electrode on said insulating layer, over said portion of the **channel region** and electrically isolated from said surface layer, a surface adjoining anode **region** of said first conductivity type situated in said **epitaxial** layer adjacent said

drain **region** and coupled to said drain **region,** an anode electrode connected to said anode **region,** an electrode being present to contact the substrate, characterized in that said adjacent surface adjoining drain and anode **regions** are spaced apart and in that the anode **region** is provided in a highly **doped** surface adjoining **region** of the second conductivity type.

Dwg.1/2

FS CPI EPI

L79 ANSWER 33 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1993-189790 [24] WPIX
DNN N1993-145873
TI Semiconductor circuit with improved breakdown voltage between source and drain - and has two conductors with elongated shapes and area of electrical isolation between controlled by gate of FET transistor.
DC U12
IN BUSSE, R W; RUMENNIK, V
PA (POWE-N) POWER INTEGRATIONS INC
CYC 8
PI EP 546377 A2 19930616 (199324)* EN 7p H01L029-784
R: DE FR GB IT NL SE
JP 05259454 A 19931008 (199345) H01L029-784
US 5258636 A 19931102 (199345) 7p H01L029-80
EP 546377 A3 19930929 (199509) H01L029-784
EP 546377 B1 19980311 (199814) EN 7p H01L029-772
R: DE FR GB IT NL SE
DE 69224709 E 19980416 (199821) H01L029-772
AB EP 546377 A UPAB: 19931116
The semiconductor comprises a first conductor (52) having an elongated shape with at least one broadside and a tip with a second conductor (58) in proximity to the first with an area of electrical isolation (60) between them at a maximum between the tip and second conductor.

The area of electrical isolation is under between the tip and the second conductor and can withstand a higher stand off voltage between the tip and the second conductor before breaking down. The circuit consists of an FET transistor (50).

The two conductors are respectively a source structure and a drain structure with the area of isolation being a **channel** which is controlled by a gate with the **channel** wider proximate to the tip than it is proximate to a broad **side**.

ADVANTAGE - Circuit is smaller in size with same breakdown voltage.
Dwg.3/4
ABEQ US 5258636 A UPAB: 19931220
The field effect transistor includes a source structure that **terminates** in a fingertip and includes a metal in contact with an n+diffusion and a p-diffusion in a **wall** diffusion. A drain structure interdigitates with and engulfs the source structure proximate to the fingertip and includes a metal in contact with an n+diffusion in an n-well diffusion. A gate structure is disposed on a field effect **channel** between the source and drain structures.

An extended drain including a lateral n-drift layer and an overlying p-top layer is connected to the drain structure and extended into the **channel** from the drain structure to beneath the gate structure except in an area of the **channel** proximate to the fingertip of the source structure where the extended drain is not extended into the **channel** farther than the drain structure. The breakdown voltage of the device is increased by virtue of the extended drain not extending into the **channel** proximate to the fingertip.

ADVANTAGE - Non-uniform **charge** distributions between source and drain pair of electrodes results in reduced electric field around tip by eliminating n-well junction near source-drain fingertips.
Dwg.3,4/4
ABEQ EP 546377 B UPAB: 19980406
The semiconductor comprises a first conductor (52) having an elongated shape with at least one broadside and a tip with a second conductor (58) in proximity to the first with an area of electrical isolation (60) between them at a maximum between the tip and second conductor.

The area of electrical isolation is under between the tip and the second conductor and can withstand a higher stand off voltage between the tip and the second conductor before breaking down. The circuit consists of

an FET transistor (50).

The two conductors are respectively a source structure and a drain structure with the area of isolation being a **channel** which is controlled by a gate with the **channel** wider proximate to the tip than it is proximate to a broad **side**.

ADVANTAGE - Circuit is smaller in size with same breakdown voltage.

Dwg.3/4

FS EPI

FA AB

L79 ANSWER 23 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1995-245833 [32] WPIX
DNN N1995-190898
TI **Trench**-based power MOSFET for disk drives, automotive electronics and power supplies - has **charge carrier** getter region, of thin material layer and of opposite conductivity to body region, to deplete body regions during an OFF-state to produce very low OFF-state leakage current.
DC T03 U12 X22
IN RUMENNIK, V
PA (RUME-I) RUMENNIK V
CYC 1
PI US 5430315 A 19950704 (199532)* 13p H01L029-10
ADT US 5430315 A Cont of US 1993-96049 19930722, US 1994-321579 19941011
PRAI **US 1993-96049 19930722; US 1994-321579 19941011**
IC ICM H01L029-10
ICS H01L029-78
AB US 5430315 A UPAB: 19950818

Trench MOSFET includes at least one pedestal, that functions as vertically-oriented body region, doped with first conductivity type of dopant, extending from top surface to bottom surface of MOSFET. For each pedestal, at least one gate region adjacent to **sidewall** of pedestal extends across the entire **sidewall** to control conduction of current throughout the pedestal, whereby a voltage applied to the gate region controls conductivity of the pedestal. Insulating layer is formed on **sidewall** of pedestal, between the gate region and the pedestal and at least one **charge carrier** getter region, of a second conductivity type opposite to the first conductivity type, in electrical contact with pedestal.

Between each pedestal and each **charge carrier** getter region making electrical contact, is formed a P-N junction that tends to deplete a **charge carrier** density within the pedestal,

wherein dopant concn. in each **charge carrier** getter region, a dopant concn. of each body region, width of each **charge carrier** getter region, width of each body region, thickness of each **charge carrier** getter region and thickness of each body region are selected to deplete each body region when **trench** MOSFET is in OFF-state. **Trench** MOSFET further comprises device for varying bias applied to the gate to control whether MOSFET is in OFF-state or ON-state.

ADVANTAGE - TMOSFET structures exhibit high level ON-state current and low level OFF-state current, and are simple to mfr. New structure exhibits greatly reduced parasitic capacitance compared to prior art.
Dwg.1/4
FS EPI

L79 ANSWER 26 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1994-048095 [06] WPIX
CR 1987-265698 [38]; 1989-341718 [47]; 1993-093316 [11]; 1993-377445 [47]; 1994-048096 [06]; 1996-299957 [30]; 1997-372071 [34]; 1998-494899 [42]
DNN N1994-037894
TI Recessed gate field effect power MOS device mfg. method e.g. power MOSFET, IGBT, MOS controlled thyristor - using **sidewall** spacer on **trenching** protective layer in self-aligned process to control pinched p-type base width lateral extent, with **trenching** protective layer formed by oxide on polysilicon on thin thermal oxide.
DC U11 U12
IN MEYER, T O; MOSIER, J W; PIKE, D A; TSANG, D W; TSANG, D
PA (ADPO-N) ADVANCED POWER TECHNOLOGY INC
CYC 20
PI US 5283201 A 19940201 (199406)* 21p H01L021-00
WO 9403922 A1 19940217 (199408) EN 42p H01L021-265
RW: AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
W: CA JP KP
EP 654173 A1 19950524 (199525) EN 21p H01L021-265
R: DE FR GB NL
EP 654173 A4 19960814 (199702) H01L021-00
AB US 5283201 A UPAB: 19981021
The recessed gate power MOSFET process involves using a substrate (20) including a P-body layer (26), N-drain layer (24), with e.g. an optional P+ layer (22) for an IGBT. A **trenching** protective layer formed on the substrate upper surface is patterned to define exposed areas as stripes or a matrix, and protected areas. **Sidewall** spacers (44) of predetermined thickness with inner surfaces (48) contact the protective layer **sidewalls**. A **trench** is formed in substrate areas with **sidewalls** aligned to the **sidewall** spacer outer surfaces and extending into the P-body layer to a preset depth. Gate oxide (60) is formed on the **trench walls** and gate polysilicon (62) refills the **trench** to a level near the substrate upper surface.

Oxide between **sidewall** spacers covers polysilicon Removing the protective layer exposes upper substrate surface between spacer inner surfaces. This area is doped to form a source layer over the body layer and then **trenched** to form a second **trench** having **sidewalls** aligned to the spacer inner surfaces. The second **trench** defines vertically-oriented source and body layers (86, 90) stacked along gate oxide layer to form vertical **channels** on opposite **sides** of the second **trench**.

USE/ADVANTAGE - Vertical **channel** power MOS structure; rectangular or U-shaped **groove**. Maintains both series source resistance and vertical **channel** resistance; avoids LOCOS stress.
Dwg.13/24
FS EPI

L79 ANSWER 28 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1994-006816 [01] WPIX
CR 1995-199066 [26]
DNN N1994-005595
TI High voltage transistor - has thick insulating region formed before gate region to allow 0.8 micron layer of field oxide to be grown over P-top region.
DC U12
IN GRABOWSKI, W B; RUMENNIK, V
PA (POWE-N) POWER INTEGRATIONS INC
CYC 8
PI US 5274259 A 19931228 (199401)* 10p H01L029-68
EP 618622 A1 19941005 (199438) EN 13p H01L029-06
R: DE FR GB IT NL SE
JP 06291311 A 19941018 (199501) 9p H01L029-784
ADT US 5274259 A US 1993-12045 19930201; EP 618622 A1 EP 1994-300638 19940128; JP 06291311 A JP 1993-336109 19931228
PRAI **US 1993-12045 19930201**
REP 01Jnl.Ref; EP 524030; EP 69429
IC ICM H01L029-06; H01L029-68; H01L029-784
ICS H01L027-01; H01L029-10; H01L029-40
AB US 5274259 A UPAB: 19950712
The semiconductor device has a substrate of a first conductivity type with a formed well of a second conductivity type. Within the well, an extended drain region of a first conductivity type is formed. An insulating region over the extended drain region is formed. A gate region is formed on a surface of the substrate. A first side of the gate region is adjacent to a first end of the extended drain region.

A drain region of the first conductivity type is formed. The drain region is in contact with a second end of the extended drain region. A source region is formed on a second side of the gate region.

USE/ADVANTAGE - Amplifiers, power converters, instrumentation. Maintains balance **compensating** charge without detrimentally affecting breakdown voltage.
Dwg.1/9
Dwg.1/9
FS EPI

L79 ANSWER 52 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1980-D9392C [18] WPIX
CR 1983-E0599K [12]
TI Power MOS FET system structure - uses high blocking voltage and has low switching resistance attained by common **region** of relatively higher conductivity (NL 15.4.80).
DC U12
IN HERMAN, T; LIDOW, A; RUMENNIK, V
PA (INRC) INT RECTIFIER CORP; (LIDO-I) LIDOW A; (HERM-I) HERMAN T
CYC 16

GB 2033658	B	19830302	(198309)		
US 4376286	A	19830308	(198312)	11p	
US 5130767	A	19920714	(199231)	8p	H01L029-78
US 5008725	B	19930112	(199305)	3p	H01L029-10
US 5191396	A	19930302	(199311)	11p	H01L029-78
US 4376286	B	19930720	(199330)	3p	H01L029-78
US 4959699	B	19931012	(199342)#	3p	H01L029-10
US 5338961	A	19940816	(199432)	13p	H01L029-76
US 4705759	B1	19950214	(199512)	1p	H01L021-265
JP 07169950	A	19950704	(199535)	10p	H01L029-78
US 5191396	B1	19951226	(199606)	2p	H01L029-78
US 5598018	A	19970128	(199710)	12p	H01L029-76
US 5742087	A	19980421	(199823)	13p	H01L029-76
US 4642666	B1	19981027	(199850)#		H01L029-76
US 4959699	B2	19990119	(199911)		H01L029-76
US 5008725	C2	20010501	(200138)		H01L029-76
US 5130767	C1	20010814	(200150)		H01L029-78

AB DE 2940699 A UPAB: 19980610
The high power MOSFET includes a semiconductor wafer having a relatively lightly **doped** major body portion for receiving junctions and being **doped** with impurities of one conductivity type. At least two spaced base **regions** of opposite conductivity are formed in wafer to a first depth. The **space** between the base **regions** defines a common conduction **region** at a given first semiconductor surface location. Two source **regions** are formed in each pair of the base **regions**, and are laterally spaced along the first semiconductor surface to define two **channel** **regions**, and are connected to respective electrodes. A gate insulation layer is disposed at least on the two **channel** **regions**. A drain conductive **region** is sepd. from the common **region** by the relatively lightly **doped** major body portion.

The common **region** is relatively highly **doped**, and extends from the given first semiconductor surface location to a depth greater than the depth of the source **region**. The resistance to current flow at the junctions between the **channel** **regions** and the common **region** and between the common **region** and the relatively lightly **doped** major body portion is reduced.

ADVANTAGE - **Epitaxially** deposited semiconductor material immediately adjacent and beneath the gate and in source-drain path has relatively high conductivity, reducing on-resistance without effecting breakdown voltage. Impurities for defining source **regions** are applied in single step.

ABEQ US 4376286 B UPAB: 19931118
A high power MOSFET is disclosed in which two laterally spaced sources each supply current through respective **channels** in one surface of a semiconductor chip which are controlled by the same gate. The **channels** lead from the source electrodes to a relatively low resistivity **region** and from there to a relatively high resistivity **epitaxially** formed **region** which is deposited on a high conductivity substrate. The drain electrode may be

either on the opposite surface of the chip or laterally displaced from and on the same **side** as the source **regions**. The **epitaxially** deposited semiconductor material immediately adjacent and beneath the gate and in the path from the sources to the drain has a relatively high conductivity, thereby to reduce the on-resistance of the device without affecting the breakdown voltage of the device. The breakdown voltage of the device is increased by forming a relatively deep P-type diffusion with a large radius in the N-type **epitaxial** layer beneath each of the sources.
Dwg.1/1

ABEQ US 4959699 B UPAB: 19931202
The high power MOSFET has two laterally spaced sources each supplying current through respective **channels** in one surface of a semiconductor chip which are controlled by the same gate. The **channels** lead from the source electrodes to a relatively low resistivity **region** and from there to a relatively high resistivity eqitaxially formed **region** which is deposited on a high conductivity substrate. The drain electrode may be either on the opposite surface of the chip or laterally displaced from and on the same **side** as the source **regions**.

The **epitaxially** deposited semiconductor material immediately adjacent and beneath the gate and in the path from the sources to the drain has a relatively high conductivity, to reduce the on-resistance of the device without effecting the breakdown voltage of the device.

ADVANTAGE - Breakdown voltage of device is increased by forming relatively deep P-type diffusion with large radius in N-type **epitaxial** layer beneath each of sources.
Dwg.1/1

ABEQ US 5338961 A UPAB: 19940928
The high power MOSFET includes a semiconductor wafer having a relatively lightly **doped** major body portion for receiving junctions and being **doped** with impurities of one conductivity type. At least two spaced base **regions** of opposite conductivity are formed in wafer to a first depth. The **space** between the base **regions** defines a common conduction **region** at a given first semiconductor surface location. Two source **regions** are formed in each pair of the base **regions**, and are laterally spaced along the first semiconductor surface to define two **channel** **regions**, and are connected to respective electrodes. A gate insulation layer is disposed at least on the two **channel** **regions**. A drain conductive **region** is sepd. from the common **region** by the relatively lightly **doped** major body portion.

The common **region** is relatively highly **doped**, and extends from the given first semiconductor surface location to a depth greater than the depth of the source **region**. The resistance to current flow at the junctions between the **channel** **regions** and the common **region** and between the common **region** and the relatively lightly **doped** major body portion is reduced.

ADVANTAGE - **Epitaxially** deposited semiconductor material immediately adjacent and beneath the gate and in source-drain path has relatively high conductivity, reducing on-resistance without effecting breakdown voltage. Impurities for defining source **regions** are applied in single step.
Dwg.2/10

ABEQ US 4705759 B UPAB: 19950328
In the high power MOSFET, two laterally spaced sources each supply current through respective **channels** in one surface of a semiconductor chip which are controlled by the same gate. The **channels** lead from the source electrodes to a relatively low resistivity **region**

and from there to a relatively high resistivity **epitaxially** formed **region** which is deposited on a high conductivity substrate. The drain electrode may be either on the opposite surface of the chip or laterally displaced from and on the same **side** as the source **regions**.

The **epitaxially** deposited semiconductor material immediately adjacent and beneath the gate and int he path from the sources to the drain has a relatively high conductivity, thereby to substantially reduce the on-resistance o the device without effecting the breakdown voltage of the device. The breakdown voltage of the device is substantially increased by forming a relatively deep p-type diffusion with a large radius in the n-type **epitaxial** layer beneath each of the sources.

Dwg.1/1

ABEQ US 5191396 B UPAB: 19960212

The high power MOSFET has two laterally spaced sources which each supply current through respective **channels** in one surface of a semiconductor chip which are controlled by the same gate. The **channels** lead from the source electrodes to a relatively low resistivity **region** and from there to a relatively high resistivity **epitaxially** formed **region** which is deposited on a high conductivity substrate. The drain electrode may be either on the opposite surface of the chip or laterally displaced from and on the same **side** as the source **regions**. The **epitaxially** deposited semiconductor material immediately adjacent and beneath the gate and in the path from the sources to the drain has a relatively high conductivity, thereby to substantially reduce the on-resistance of the device without effecting the breakdown voltage of the device. The breakdown voltage of the device is substantially increased by forming a relatively deep p-type diffusion with a large radius in the n-type **epitaxial** layer beneath each of the sources.

Dwg.1/1

ABEQ US 5598018 A UPAB: 19970307

A three-**terminal** power metal oxide silicon field effect transistor device comprising:

a wafer of semiconductor material having first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly **doped** major body portion for receiving junctions and being **doped** with impurities of one conductivity type;

at least first and second spaced base **regions** of the opposite conductivity type to said one conductivity type formed in said wafer and extending from said first semiconductor surface to a depth beneath said first semiconductor surface; the **space** between said at least first and second base **regions** defining a common conduction **region** of one conductivity type at a given first semiconductor surface location;

first and second source **regions** of said one conductivity type formed in said at least first and second base **regions**, respectively, at first and second first surface locations and extending from said first and second first surface locations to a depth less than said depth of said base **regions**; said first and second source **regions** being laterally spaced along said first semiconductor surface from the facing respective edges of said common conduction **region** thereby to define first and second **channel** **regions** along said first semiconductor surface between each of said first and second source **regions**, respectively, and said common conduction **region**;

source electrode means connected to said source **regions** and comprising a first **terminal**;

gate insulation layer means on said first surface, disposed at least on said first and second **channel regions**;

gate electrode means on said gate insulation layer means, overlying said first and second **channel regions** and comprising a second **terminal**;

a drain electrode connected to said first surface and comprising a third **terminal**;

each of said at least first and second spaced base **regions** of said opposite conductivity type having respective profiles which include relatively shallow depth **regions** extending from said common **region** and underlying their said respective first and second source **regions**, and respective relatively deep, relatively large radius **regions** extending from said shallow depth **regions** which are laterally spaced from beneath said respective source **regions** on the **side** of said source **regions** which is away from said common **region**.

Dwg.8/10

FS EPI

L79 ANSWER 35 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1993-076777 [09] WPIX
CR 1995-338548 [44]; 1997-031559 [03]
DNN N1993-058984 DNC C1993-033878
TI Mfg. vertical MOSFET for **integrated** circuit - by decreasing size of unit cell and on-resistance per unit area, useful as MOS IC for electric power switching elements etc..
AW **INTEGRATED** CIRCUIT.
DC L03 U11 U12
IN TAKAHASHI, S; TOKURA, N; KATAOKA, M; YAMAMOTO, T
PA (NPDE) DENSO CORP; (NPDE) NIPPONDENSO CO LTD; (IPIC-N) IPICS CORP
CYC 16
PI WO 9303502 A1 19930218 (199309)* JA 46p H01L029-784
RW: AT BE CH DE DK ES FR GB GR IT LU MC NL SE
W: JP US
EP 550770 A1 19930714 (199328) EN 22p H01L029-784
R: DE FR GB
JP 05503460 X 19930701 (199331) 2p H01L029-784
EP 550770 A4 19930825 (199527) H01L029-784
US 5460985 A 19951024 (199548) 19p H01L021-8232
EP 550770 B1 19971112 (199750) EN 34p H01L029-772
R: DE FR GB
DE 69223128 E 19971218 (199805) H01L029-772
US 6015737 A 20000118 (200011) H01L021-336
AB WO 9303502 A UPAB: 20000301
Producing a vertical MOSFET (Metal Oxide Semiconductor Field Effect Transistor) comprises (1) a first conductive semiconductor layer contg. lower impurities than the substrate is formed on the main surface of a semiconductor substrate, (2) selective oxidn. process in which a predetermined region of the main surface of the semiconductor layer is selectively oxidised with a predetermined depth so as to form a selective oxidn. film. (3) Impurity introduction process in which in order to form a **channel** on the surface of the semiconductive surface adjacent to the **side** surface of the selective oxidn. film, impurities of the second conductive type and of the first conductive type are doubly diffused in this order with self alignment to the selective oxidn. film.

By this double diffusion the length of the **channel** is determined, and also the base layer of the second conductive type and the source layer of the first conductive type are formed. (4) Gate formation process in which a **groove** structure having a predetermined depth is formed by removing the selective oxidn. film, the inside **wall** of the **groove** including the part to be the **channel** is oxidised so as to form the gate oxidn. film, and the gate electrode is formed on the gate oxidn. film. (5) Source and drain electrode formation process: The source electrode which is electrically connected to both the source layer and the base layer, and the drain electrode which is electrically connected to the other main surface of the semiconductor base, are formed.

USE/ADVANTAGE - In the vertical MOSFET the depth of the U-**groove** can be minimised because there is no need to form a deeper **groove** than necessary in anticipation of positional discrepancy. Hence the size of the unit cell can be decreased dramatically. The on-resistance per unit area can also be decreased. The MOSFET is very useful as a MOSIC for electrode power switches etc.
Dwg.1/23
ABEQ EP 550770 A UPAB: 19931116
Prodn. comprises (1) forming a first conductive semiconductor laye contg. lower impurities than the substrate on the main surface of semiconductor substrate; (2) selectively oxidising predetermined region of the main surface of the semiconductor layer is selectively oxidised with predetermined depth so as to form a selective oxidn. film; and (3) introducing impurity in order to form **channel** on the surface of

the semiconductive surface adjacent to the **side** surface of the selective oxidn. film. Impurities of the second conductive type and of the first conductive type are doubly diffused in this order with self alignment to the selective oxidn. film; (4) forming gate in which **groove** structure having predetermined depth is formed by removing the selective oxidn. film, the inside **wall** of the **groove** including the part to be **channel** is oxidised so as to form the gate oxidn. film, and the gate electrode is formed on the gate oxidn. film; and (5) forming source and drain electrode. The source electrode which is electrically connected to both the source layer and the base layer, and the drain electrode which is electrically connected to the other main surface of the semiconductor base, are formed.

USE/ADVANTAGE - Used in the vertical MOSFET the depth of the U-**groove** can be minimised because there is no need to form a deeper **groove** than necessary in anticipation of positional discrepancy. Hence the size of the unit cell can be decreased dramatically. The on-resistance per unit area can also be decreased. The MOSFET is very useful as a MOSIC for electrode power switches, etc..
Dwg.1/23

ABEQ JP 05503460 X UPAB: 19931118

Producing a vertical MOSFET comprises (1) a first conductive semiconductor layer contg. lower impurities than the substrate is formed on the main surface of a semiconductor substrate, (2) selective oxidn. process in which a predetermined region of the main surface of the semiconductor layer is selectively oxidised with a predetermined depth so as to form a selective oxidn. film. (3) Impurity introduction process in which in order to form a **channel** on the surface of the semiconductive surface adjacent to the **side** surface of the selective oxidn. film, impurities of the second conductive type and of the first conductive type are doubly diffused in this order with self alignment to the selective oxidn. film.

By this double diffusion the length of the **channel** is determined, and also the base layer of the second conductive type and the source layer of the first conductive type are formed. (4) Gate formation process in which a **groove** structure having a predetermined depth is formed by removing the selective oxidn. film, the inside **wall** of the **groove** including the part to the **channel** is oxidised so as to form the gate oxidn. film, and the gate electrode is formed on the gate oxidn. film. (5) Source and drain electrode formation process: The source electrode which is electrically connected to both the source layer and the base layer, and the drain electrode which is electrically connected to the other main surface of the semiconductor base, are formed.

USE/ADVANTAGE - In the vertical MOSFET the depth of the U-**groove** can be minimised because there is no need to form a deeper **groove** than necessary in anticipation of positional discrepancy. Hence the size of the unit cell can be decreased dramatically. The on-resistance per unit area can also be decreased. The MOSFET is very useful as a MOSIC for electrode power switches etc.
Dwg.0/1

ABEQ US 5460985 A UPAB: 19951204

A vertical type MOSFET is mfd. by (a) forming a 1st conductivity type semiconductor layer having a (III) oriented surface on a 1st conductivity type substrate having a higher impurity concn.; (b) forming a local oxide film on the semiconductor layer and contacting it in a (100) crystal plane; (c) forming a base layer by diffusing 2nd type impurities in the semiconductor layer, self-aligned w.r.t. the local oxide film; (d) forming a source layer by diffusing the 1st type impurities in the semiconductor layer; (e) forming a **groove** structure including a **channel** by removing the local oxide film; (f) forming a gate oxide film thicker at the **groove** bottom than at the **groove** **side**, by oxidising; (g) forming a gate electrode on the gate oxide

film; (h) forming a source electrode in electrical contact with the source and base layers, and (i) forming a drain electrode in contact with a 2nd face of the substrate.

ADVANTAGE - **Groove** formation before formation of base and source layers. High prodn. yield and reliability.
Dwg.1/23

ABEQ EP 550770 B UPAB: 19971217
A production method of a vertical type MOSFET comprising the steps of: preparing a semiconductor substrate (1); forming a semiconductor layer (2) of a first conductivity type at one main face **side** of the semiconductor substrate (1), the semiconductor layer (2) having an impurity concentration lower than that of the semiconductor substrate (1) and having a main surface; locally oxidizing a predetermined region of the main surface of the semiconductor layer (2) to form a local oxide film (65) eroding the main surface of the semiconductor layer (2) by a predetermined depth in the predetermined region; forming **channels** (5) on the semiconductor layer (2) surface contacting a **side** face (54) of the local oxide film (65) by double diffusing impurities of the second conductivity type and the first conductivity type from the main surface successively in a manner of self-alignment with respect to the local oxide film (65); whereby the length of the **channel** (5) is determined by the double diffusion and simultaneously with it a base layer (16) of the second conductivity type and a source layer (4) of the first conductivity type are formed; removing the local oxide film (65) after the double diffusion to form a **groove** structure (50) having the predetermined depth; oxidizing an inner **wall** (51) of the **groove** structure (50) including a portion to become the **channel** (5) to provide a gate oxide film (8); forming a gate electrode (9) on the gate oxide film (8); forming a source electrode (19) electrically contacting both the source layer (4) and the base layer (16); and forming a drain electrode (20) electrically contacting the other main face **side** of the semiconductor substrate (1), the production method of a vertical type MOSFET being characterized in that: the semiconductor layer (2) forming step includes a step of forming a silicon layer, an index of plane of the main surface of which is (111) or about (111); the local oxidizing step includes a step of controlling an index of plane of the semiconductor layer (2) surface contacting the **side** face (54) of the local oxide film (65) to be (100) or about (100); and in that: the step of removing the local oxide film (65) to form the **groove** structure (50) is performed in such a manner that an index of plane of the bottom face (53) of the **groove** structure (50) is (111) or about (111) and an index of plane of the **side** face (54) of the **groove** structure (50) is (100) or about (100).
1a,1b/23

FS CPI EPI
FA AB; GI

L79 ANSWER 29 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1993-381172 [48] WPIX
DNN N1995-127095 DNC C1995-075056
TI Power DMOS with improved current detection accuracy - comprises first conductivity type substrate, main current section and emulation current section.
DC L03 U11 U12
IN KUROYANAGI, A; NISHIZAWA, T; TSUZUKI, Y
PA (NPDE) NIPPONDENSO CO LTD
CYC 2
PI JP 05283705 A 19931029 (199348)* 7p H01L029-784
US 5410171 A 19950425 (199522)B 13p H01L029-10
US 5534454 A 19960709 (199633) 12p H01L021-265
ADT JP 05283705 A JP 1992-74534 19920330; US 5410171 A US 1993-38951 19930329; US 5534454 A Div ex US 1993-38951 19930329, US 1995-385553 19950208
FDT US 5534454 A Div ex US 5410171
PRAI **JP 1992-74534 19920330**
IC ICM H01L021-265; H01L029-10; H01L029-784
ICS H01L021-70; H01L027-00; H01L027-02; H01L029-78
AB US 5410171 A UPAB: 19950609 ABEQ treated as Basic
Semiconductor device has: (a) first conductivity type substrate; (b) main current section including main well **regions** of second type, first source **region** of first type, main gate electrode on the surface of a **channel region** through a gate insulation film the **channel** being formed in a **region** located between the first source **region** and the substrate surface; and (c) emulation current section including sub well **regions** of second type, second source of first type, sub gate electrode formed on a **channel** through gate insulation film the **channel** being formed in a **region** located between the second source and the substrate where the subgate electrode is controlled by a gate voltage the level of which is identical to that of the main gate electrode, an insulation film formed on the substrate between the main current and emulation current sections and thicker than the gate insulation film, a line well **region** of second type formed on the substrate on a **side** facing the emulation current section with respect to the insulation film being formed so as to encircle the emulation section. The subgate electrode has an opening for forming subwell **regions** and a peripheral portion used as an opening for forming the line well **region** and for positioning it apart from the sub well.

Substrate (1) was n+Si with a common drain electrode (93) source electrode (92,91). **Epitaxial** layer (2) p-well (31) annular well (32) and main wells (41,42,43) sources (51,52) contact electrode (71,72) of **doped** polysilicon, gate insulation (81) and thick silicon oxide (82) and insulation (83).

USE - Power DMOS devices.

ADVANTAGE - Improved current detection accuracy using standard processing.
Dwg.1/14
AB JP 05283705 A UPAB: 19971105
Dwg.1/14
Dwg.1/14
ABEQ US 5534454 A UPAB: 19960823
A method for producing a semiconductor device, comprises: (a) forming an **epitaxial** layer on a semiconductor substrate of a first conduction type; (b) forming a gate insulation film over the semiconductor substrate, forming a main gate electrode and a sub-gate electrode on the gate insulation film, and forming a line opening between the main gate electrode and the sub-gate electrode; (c) **doping** the surface of the **epitaxial** layer with impurities with at least the main gate electrode and the sub-gate electrode serving as masks, to form main wells reaching under the main gate electrode, sub-wells reaching under the

sub-gate electrode, and a line well, which is independent of the main wells and surrounds the sub-wells with a distance away from the sub-wells; and (d) **doping** the surfaces of the main wells and the sub-wells with impurities with at least the main gate electrode and the sub-gate electrode serving as masks, to form sources of the first conduction type for a main current section and a detective section, the sources being shallower and narrower than the main wells and the sub-wells and reaching under the main gate electrode and the sub-gate electrode.
Dwg.0/14

FS CPI EPI

L79 ANSWER 34 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1993-093316 [11] WPIX
CR 1987-265698 [38]; 1989-341718 [47]; 1993-377445 [47]; 1994-048095 [06]; 1994-048096 [06]; 1996-299957 [30]; 1997-372071 [34]; 1998-494899 [42]
DNC C1993-041231
TI IGBT-type 4-layer power device structure on silicon substrate - for high voltage solid state power switches, conducting and switching high current and voltages at high speed.
AW INSULATED GATE BIPOLAR TRANSISTOR.
DC L03
IN KATANA, J M; PIKE, D A; SDRULLA, D; TSANG, D W
PA (ADPO-N) ADVANCED POWER TECHNOLOGY INC
CYC 21
PI US 5190885 A 19930302 (199311)* 34p H01L021-00
WO 9305535 A1 19930318 (199312) EN 115p H01L021-467
RW: AT BE CH DE DK ES FR GB GR IE IT LU MC NL SE
W: CA JP KR
TW 201849 A 19930311 (199330) H01L021-00
EP 601093 A1 19940615 (199423) EN H01L021-467
R: CH DE FR GB LI
JP 06510400 W 19941117 (199505) H01L029-784
EP 601093 A4 19950412 (199613) H01L021-00
EP 601093 B1 20020306 (200219) EN H01L021-22
R: CH DE FR GB LI
EP 1182706 A2 20020227 (200222) EN H01L029-06
R: CH DE FR GB LI
EP 1182707 A2 20020227 (200222) EN H01L029-10
R: CH DE FR GB LI
DE 69232461 E 20020411 (200232) H01L021-22
AB US 5190885 A UPAB: 20020521
An improved fabrication process for making a MOS-type insulated gate controlled 4-layer power switching device, comprises: forming a semiconductor substrate having a first layer of a first dopant type defining a device anode and second layer of a second, opposite-polarity dopant type defining a drain region extending from an upper surface of the substrate toward the first layer; forming an insulative layer on the upper surface of the second layer of the substrate and an insulated gate contact layer on the insulative layer; forming double diffused regions including a body region of the first dopant type and a source region of the second dopant type within the body region, the body region forming 2 PN junctions with the drain and source regions, respectively spaced apart so as to define a **channel** region in the body region subjacent the insulated gate contact; forming a source contact alongside the gate contact but spared insulatively therefrom, the source contact forming an electrical connection to the source region and the body region and a short therebetween and defining a cathode contact for the device; forming a anode contact on the opposite **side** of the substrate in electrical connection to the first layer; forming the second layer including: forming a first portion contacting the first layer and having a first thickness and a first doping concn.; forming a second portion contacting the second layer and extending to the upper surface to receive the double diffused regions; sizing and doping the second portion to a second thickness and a second doping concn. sufficient to block a predetermined max. reverse bias voltage; sizing and doping the first portion to produce a predetermined output impedance (Ro) sufficient to resist current flow during forward conduction when a high voltage (Vce) is across the cathode and anode contacts.
USE/ADVANTAGE - Improved process for making 4-layer (PNPN) devices, e.g. IGTs, IGBTs, MCTs, emitter controlled thyristors, and other gate controlled minority **carrier** devices, as well as power MOSFET devices, on a Si substrate.
Dwg.2/28

L79 ANSWER 30 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1993-377445 [47] WPIX
CR 1987-265698 [38]; 1989-341718 [47]; 1993-093316 [11]; 1994-048095 [06]; 1994-048096 [06]; 1996-299957 [30]; 1997-372071 [34]; 1998-494899 [42]
DNN N1993-291440 DNC C1993-167629
TI IGBT power device structure - for high voltage solid state power, switches operating at high speed without parasitic effects.
DC L03 U11 U12
IN KATANA, J M; PIKE, D A; TSANG, D W
PA (ADPO-N) ADVANCED POWER TECHNOLOGY INC
CYC 1
PI US 5262336 A 19931116 (199347)* 32p H01L021-00
ADT US 5262336 A CIP of US 1986-842771 19860321, Div ex US 1988-194874 19880517, Cont of US 1989-439101 19891116, Cont of US 1990-467636 19900119, CIP of US 1991-737560 19910726, Cont of US 1991-751441 19910828, US 1992-852932 19920313
FDT US 5262336 A CIP of US 4748103, Div ex US 4895810, Cont of US 5045903, CIP of US 5182234
PRAI US 1991-751441 19910828; **US 1986-842771 19860321; US 1988-194874 19880517; US 1989-439101 19891116 ; US 1990-467636 19900119; US 1991-737560 19910726**; US 1992-852932 19920313
IC H01L021-02; H01L021-467
ICM H01L021-00
ICS H01L021-02; H01L021-467
AB US 5262336 A UPAB: 19981021
Fabrication process for making a MOS-type insulated gate controlled 4-layer power switching device comprises: forming a semiconductor substrate having a first layer of a first dopant type defining a device anode and a second layer of a second, opposite-polarity dopant type defining a drain region extending from an upper surface of the substrate toward the first layer, forming an insulative layer on the upper surface of the second layer of the substrate and an insulated gate contact layer on the insulative layer, forming double diffused regions including a body region of the first dopant type and a source region of the second dopant type within the body regions, the body region forming 2 PN junctions with the drain and source regions, respectively spaced apart so as to define a **channel** region in the body region subjacent the insulated gate contact; forming a source contact alongside the gate contact but spaced insulatively therefrom, the source contact forming an electrical connection to the source region and the body region and a short therebetween and defining a cathode contact for the device, forming an anode contact on the opposite **side** of the substrate in electrical connection to the first layer, formign the second layer includes, forming a first portion contacting the first layer and having a first thickness and a first doping concn. forming a second portion contacting the second layer and extending to the upper surface to receive the double diffuse regions, sizing and doping the second portion to a second thickness and a second doping concn. sufficient to block a predetermined max. reverse bias voltage, sizing and the final portion to produce a predetermined output impedance (Ro) sufficient to resist current flow during forward conduction when a high voltage (Vce) is across the cathode and anode contacts.

USE/ADVANTAGE - Improved process for making 4-layer (PNPN) devices such as IGT or IGBT, MCTs, emitter controlled thyristors and other gate controlled minority **carrier** devices, as well as power MOSFET devices, on a Si substrate. Improvements include forward conduction, reverse bias blocking, turn-off time and control of suseptibility of latching and other breakdown conditions.
FS CPI EPI

L79 ANSWER 31 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1993-302798 [38] WPIX
DNN N1993-232872
TI Temp. **compensated** overcurrent and undercurrent detector - monitors current through solenoid or other load and signals when load current falls outside upper or lower limits, which may indicate failure of other circuit supplying load current.
DC S01 T04 U11 U12 U13 U24
IN ASHLEY, D J; DEMOOR, M K
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 5245261 A 19930914 (199338)* 26p H01L029-73
ADT US 5245261 A US 1991-782211 19911024
PRAI **US 1991-782211 19911024**
IC ICM H01L029-73
ICS H01L023-58
AB US 5245261 A UPAB: 19931123

The circuit for detecting overcurrent and/or undercurrent conditions, includes a load transistor having an on-resistance which passes load current and varies with temp. A pilot transistor is integrated with the load transistor such that as it heats up due to the load current, and heats up due to heat conduction from the load transistor. The pilot transistor has an on-resistance which varies proportionally or similarly to that of the load transistor as it heats-up due. A detector senses a voltage across the on-resistance of the load transistor corresp. to the load current.

A device, including a current source coupled to the on-resistance of the pilot transistor, generates a reference voltage either above or below an acceptable range of sensed voltages representing an acceptable range of load currents. The reference voltage is **compensated** for temp. effects on the on-resistance of the load transistor. The reference voltage above the acceptable range represents an overcurrent reference and the reference voltage below the acceptable range represents an undercurrent reference. A comparator generates either an overcurrent signal when the sensed voltage is greater than the reference voltage when it is an overcurrent reference, or an undercurrent signal when the sensed voltage is less than the reference voltage while it is an undercurrent reference.

ADVANTAGE - Provides detection window for two levels of drive current with minimum amount of circuitry.

16

L79 ANSWER 32 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1993-214419 [26] WPIX
DNN N1993-164789 DNC C1993-095165
TI Vertical insulated gate semiconductor device mfr. - comprises diffusing arsenic into upper surface of n-type epitaxial layer, forming p-type base region and n-plus type source layer by diffusion self-alignment technique, etc..
DC L03 U11 U12
IN OKABE, N; TOKURA, N
PA (NPDE) NIPPONDENSO CO LTD; (NPDE) DENSO CORP
CYC 18
PI WO 9312545 A1 19930624 (199326)* JA 39p H01L029-784
RW: AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
W: US
JP 05160407 A 19930625 (199330) H01L029-784
EP 570595 A1 19931124 (199347) EN 27p H01L029-784
R: DE FR GB
US 5545908 A 19960813 (199638) 23p H01L029-78
EP 570595 B1 19980311 (199814) EN 30p H01L029-772
R: DE FR GB
DE 69224740 E 19980416 (199821) H01L029-772
AB WO 9312545 A UPAB: 19931116
Arsenic is diffused in advance into the uppermost surface of an n- type epitaxial layer (2) to form a gate oxide film (3) and gate electrodes (4). Then, a p-type base region (8) and an n+ type source layer (7) are formed by a DSA technique and double diffusion in a self-alignment manner with the gate electrode (4). Hence, in the uppermost surface, the junction depth of the p-type base regions (8) in the lateral direction is **compensated**, and the channel length of channels (9) is shortened substantially. Also, when a threshold voltage is designed in the same manner as conventionally designed, it is possible to make the impurity density of the p-type base region (8) higher by the amt. of the impurity density of the arsenic in the uppermost surface. Thus, the resistance value of p-type pinch layer (14) formed directly under the n+ source layer (7) of the p-type base region (8) can be reduced by the amt.
Dwg.1/14
ABEQ EP 570595 A UPAB: 19940111
Arsenic is diffused in advance into the uppermost surface of an n- type epitaxial layer (2) to form a gate oxide film (3) and gate electrodes (4). Then, a p-type base region (8) and an n+ type source layer (7) are formed by a DSA technique and double diffusion in a self-alignment manner with the gate electrode (4). Hence, in the uppermost surface, the junction depth of the p-type base regions (8) in the lateral direction is **compensated**, and the channel length of channels (9) is shortened substantially. Also, when a threshold voltage is designed in the same manner as conventionally designed, it is possible to make the impurity density of the p-type base region (8) higher by the amt. of the impurity density of the arsenic in the uppermost surface. Thus, the resistance value of p-type pinch layer (14) formed directly under the n+ source layer (7) of the p-type base region (8) can be reduced by the amt.
Dwg.1/22
ABEQ US 5545908 A UPAB: 19960924
A vertical type insulated-gate semiconductor device comprising: a semiconductor substrate having a first impurity concentration; a semiconductor layer of a first conductivity type and having a second impurity concentration lower than the first impurity concentration of the semiconductor substrate, the semiconductor layer being located on the semiconductor substrate; an insulated gate structure located on a main surface of the semiconductor layer, the insulated gate structure including a gate electrode; a well region of a second conductivity type having a first vertical diffusion depth; a source region of the first conductivity type formed within the well region, the well region and the source region

being double-diffused laterally from an edge of the gate electrode into the main surface of the semiconductor layer below the gate electrode to thereby align a channel in a vicinity of the edge of the gate electrode, the channel being located at a surface of the well region below the gate electrode; a diffusion layer of the first conductivity type formed at the main surface of the semiconductor layer so as to overlap the channel, the diffusion layer having a third impurity concentration higher than the second impurity concentration of the semiconductor layer and a second vertical diffusion depth shallower than the first vertical diffusion depth of the well region, a net amt. of a first impurity density of the first conductivity type of the diffusion layer being higher than a net amt. of a second impurity density of the second conductivity type of the surface of the well region where the channel is formed; a **compensated** region of the first conductivity type formed below the gate electrode and at the main surface of the semiconductor layer proximate to the well region, the **compensated** region eroding a configuration of the well region at the main surface of the semiconductor layer and below the gate electrode; and a length of the channel being determined by a distance between the source region and the **compensated** region.
Dwg.0/22

ABEQ EP 570595 B UPAB: 19980406
Arsenic is diffused in advance into the uppermost surface of an n- type epitaxial layer (2) to form a gate oxide film (3) and gate electrodes (4). Then, a p-type base region (8) and an n+ type source layer (7) are formed by a DSA technique and double diffusion in a self-alignment manner with the gate electrode (4). Hence, in the uppermost surface, the junction depth of the p-type base regions (8) in the lateral direction is **compensated**, and the channel length of channels (9) is shortened substantially. Also, when a threshold voltage is designed in the same manner as conventionally designed, it is possible to make the impurity density of the p-type base region (8) higher by the amt. of the impurity density of the arsenic in the uppermost surface. Thus, the resistance value of p-type pinch layer (14) formed directly under the n+ source layer (7) of the p-type base region (8) can be reduced by the amt.
Dwg.1/22

FS CPI EPI

L79 ANSWER 38 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1990-335101 [44] WPIX
DNN N1990-256148
TI **Trench** JFET **integrated** circuits - has first **trench** forming gate and conductive layer applied to surface giving P-N junction with added capacitance.
DC S03 U11 U12 U13
IN SOLOMON, A L
PA (NOTH) NORTHROP GRUMMAN CORP; (GRUA) GRUMMAN AEROSPACE CORP
CYC 16
PI WO 9012421 A 19901018 (199044)* 29p
RW: AT BE CH DE DK ES FR GB IT LU NL SE
W: JP KR
CA 2009068 A 19901003 (199051)
US 5010025 A 19910423 (199120) 9p
US 5122851 A 19920616 (199227) 9p H01L027-14
CA 2009068 C 19990126 (199915) H01L029-808

AB WO 9012421 A UPAB: 19930928
The production of Junction Field Effect **integrated** circuit elements formed on silicon wafer and used to interface circuits such as infrared detectors to a processing network to amplify, store and detect signals.

A first **trench** (41) in the substrate (20) formign a gate **channel** (45) forms a conductive **channel**. The conductive layer interfaces with the gate **channel** to form a P-N junction. Source and drain regiosn are adjacent. An integral capacitor may be added to the construction by forming a second **trench** (51) wich extends through and excavates a portion of the first **trench**. A layer of insulating material is then applied.

ADVANTAGE - Minimises circuit noise.
8/18

ABEQ US 5010025 A UPAB: 19930928
The method comprises a step of forming a first **trench** in a semiconductor substrate, forming a gate **channel** about the **trench** and forming a conductive layer upon the surface of the gate **channel**. The conductive layer interfaces with the gate **channel** to form a p-n junction. Source and drain regions are formed adjacent to a **trench** and disposed in electrical contact with the gate **channel**.

An integral capacitor may be added to the construction by forming a second **trench**, which extends through and excavates a portion of the first **trench**. The drain region is extended about the surface of the second **trench** to remain in electrical contact with the gate **channel**. A layer of insulating material is applied to the second **trench**, which is then filled with a body of conductive material. The conductive material is insulated from the conductive layer by the insulating layer.

USE - To form **trench** gate JFET transistor.

ABEQ US 5122851 A UPAB: 19930928
A **trench** gate JFET comprises a first **trench** formed in a semiconductor substrate of a first conductive type, the first **trench** being of sufficient depth to mitigate the generation of 1/f noise. A gate **channel** of the first conductivity type is formed about the first **trench**. A conductive layer formed of a second conductivity type within the first **trench** upon the gate **channel**.

Source and drain regions of the first conductivity type are formed upon the semiconductor substrate surface adjacent opposite **sides** of the first **trench**. A first region of doped material is formed within the substrate about the source and drain regions and the gate **channel**.

ADVANTAGE - Avoids spurious residual **charge** effects.

L79 ANSWER 39 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1989-326283 [45] WPIX
DNN N1989-248365 DNC C1989-144428
TI Symmetrical blocking high voltage breakdown semiconductor device - with a lower junction **terminal** brought to the upper surface.
DC A85 L03 U12
IN TEMPLE, V A
PA (GENE) GENERAL ELECTRIC CO; (HARO) HARRIS CORP
CYC 6
PI EP 341075 A 19891108 (198945)* EN 12p
R: DE FR IT NL
JP 02022869 A 19900125 (199010)
US 4904609 A 19900227 (199015)
US 4999684 A 19910312 (199113)
EP 341075 B1 19960417 (199620) EN 16p H01L029-866
R: DE FR IT NL
DE 68926261 E 19960523 (199626) H01L029-866
AB EP 341075 A UPAB: 19960129
Fabrication method of a symmetrical blocking, high breakdown voltage, semiconductor device is new. Mfr., with reference to the figure (1) comprises using a semiconductor substrate (14) of a first conductivity type having an epitaxial layer (16) of a second conductivity type. First and second laterally spaced regions of the first conductivity type (20, 22) are formed in an upper surface of the epitaxial layer to form repsectively first and second PN junctions. A **groove** (60) having a sloped **sidewall** is formed in the second region which extends from the upper surface, through epitaxial layer and into the substrate. Impurities of a first conductivity type are implanted into the **side walls**, of the **groove** to form a thin layer (64). The deice is annealed to activate the impurities so that the implanted layer (64) electrically connects the second region (22) to the substrate.

USE/ADVANTAGE - A simple and convenient method for bringing the reverse voltage blocking junction to a **termination** at the device surface. Complete fabrication of a plurality of devices is possible, prior to each individual die being broken out of the wafer.
1E/2
Dwg.1E/2
ABEQ US 4904609 A UPAB: 19930923
Symmetrical blocking high breakdown voltage semiconductor device is produce by firstly providing a substrate of semiconductor material of a first conductivity type having on it an epitaxial layer (I) of a second conductivity type. First and second, laterally spaced regions of the first conductivity type are formed in an upper surface of layer (I), the first and second regions forming, with layer (I), respective first and second PN junctions.

A **groove** is formed having a sloped **sidewall** in the second region, the **groove** extending from the upper surface, through the second region and layer (I), into the substrate. Impurities of the first conductivity type are implanted into the **sidewall** of the **groove**, to form a thin implanted layer of the first conductivity type. Finally, the device is annealed sufficiently to activate the impurities in the implanted layer to form a low resistivity path that electrically connects the second region to the substrate.

ADVANTAGE - The reverse voltage blocking junction in semiconductor devices contg. PNP structures is brought to the top surface of the wafer.
@@
ABEQ US 4999684 A UPAB: 19930923
Device comprises a 1st conductivity type substrate; a 2nd conductivity type epitaxial layer; a main region of 1st type extending into the epitaxial layer from its upper surface; a sec. region of 1st type extending into the epitaxial layer from its upper surface and surrounding

the main region, this sec. region spaced from the main region and having a sloped **sidewall** surface which extends from the upper surface of the epitaxial layer through the sec. region and epitaxial layer and into the substrate; the main and sec. regions forming respective PN junctions with the epitaxial layer; and a thin implanted layer of 1st type impurities in the sloped **sidewall** surface forming a low resistivity path to electrically connect the sec. region to the substrate. A means is between the main and sec. regions to control the symmetrical blocking and breakdown voltage of the device comprising a 1st junction **termination** extension comprising a 1st type region extending laterally from the main region toward the sec. region, and a 2nd junction **termination** extension comprising a 1st type region extending laterally from the sec. region toward the 1st extension. A field stop region is between each extension.

ADVANTAGE - Relatively simple construction, having symmetrical blocking and voltage breakdown characteristics. The device can be mass produced.

ABEQ EP 341075 B UPAB: 19960520

A semiconductor device comprising a semiconductor substrate (14; 88) of a first conductivity type; an epitaxial layer (16; 90) of a second conductivity type disposed on the substrate (14; 88) a main region (20; 94) of the first conductivity type extending into said epitaxial layer (16; 90) from an upper surface (18; 92) thereof; a sloped **sidewall** (62) extending from the upper surface (18; 92(of the said epitaxial layer (16; 90) through the epitaxial layer and into the substrate (14; 88); and a thin implanted layer of impurities of the first conductivity type (64,140) in the sloped **sidewall** (82), which semiconductor device is characterised by being a symmetrical blocking high breakdown voltage semiconductor device further comprising a secondary region (22; 98) of the first conductivity type extending into said epitaxial layer (16; 90) from the upper surface (18; 92) thereof and surrounding the main region (20; 94), said secondary region (22; 98) being spaced from said main region (20; 94), the sloped **sidewall** (62) extending through the secondary region (22; 98) so that the thin implanted layer of impurities of the first conductivity type (64,140) forms a low resistivity path for electrically connecting the secondary region (22; 98) to the substrate (14; 88).

Dwg.1A/2D

FS CPI EPI

FA AB

MC CPI: A12-E07C; L04-C08; L04-C11

L79 ANSWER 40 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1989-134648 [18] WPIX
DNN N1990-156668 DNC C1990-087121
TI Semiconductor IC - has FET structure to weaken electric field between source and drain areas NoAbstract Dwg 1/4.
DC U12 U13 U14
PA (MITQ) MITSUBISHI DENKI KK
CYC 2
PI JP 01080070 A 19890324 (198918)*
US 4935802 A 19900619 (199027)
ADT JP 01080070 A JP 1987-238429 19870921; US 4935802 A US 1989-418894 19891004
PRAI **JP 1987-238429 19870921**
IC H01L027-10; H01L029-78
ABEQ US 4935802 A UPAB: 19930923

IC formed on a single substrate has EPROM transistor (10) and a further transd)transistor (20) in a second area for use as a DRAM, CPU etc., thea further transistor having a gate (3,2) over a **channel**, and source and drain regions (1) sepd. from the **channel** by lower impurity layers (6). Also, the gate oxide layer (2) is thickened over the drain region **side** of the device.

ADVANTAGE - The thickened gate structure and lightly doped source and drain regions weaken the electric field between source and drain so that hot electron breakdown is avoided, even when gate length is minimised to 1.3 micron or less to obtain high **integration**. (First major country equivalent to J01080070-A)
4/4

L79 ANSWER 41 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1988-354884 [50] WPIX
DNN N1988-269101
TI High power MOS FET with **integrated** circuit - had first conductivity layer on monocrystal substrate, forming field decreasing surface region.
DC U12 U13
IN KINZER, D M
PA (INRC) INT RECTIFIER CORP
CYC 4
PI DE 3816002 A 19881208 (198850)* 13p
JP 63310175 A 19881219 (198905)
US 4866495 A 19890912 (198946) 12p
DE 3816002 C 19900215 (199007)
US 5023678 A 19910611 (199126)
IT 1217194 B 19900314 (199208)
ADT DE 3816002 A DE 1988-3816002 19880510; JP 63310175 A JP 1988-130045 19880527; US 4866495 A US 1987-54627 19870527; US 5023678 A US 1989-391487 19890809
PRAI **US 1987-54627 19870527**
IC G05F003-24; H01L023-56; H01L027-06; H01L029-78
AB DE 3816002 A UPAB: 19930923
A first layer (48) of first conductivity is formed on a moncrystalline substrate and forms a first field depletion region. In the first layer surface, away from the substrate (40), is formed a main region (53) of opposite conductivity. In both the first layer and the main region is formed a source region (56,57) i.e. spaced from the main region edge.
The source forms a surface **channel** (54,55) covered by a gate oxide (61,62) and a gate electrode (63,64). A first conductivity drain region (70) spaced laterally from the main region, is formed in the first layer surface. A second region (71) of opposite conductivity is provided in the substrate surface between the main and drain regions, and forms a second field depletion region.
USE/ADVANTAGE - For **integrated** power circuit with source and drain at HV, with all components formed in single chip.
6/13
ABEQ DE 3816002 C UPAB: 19930923
A main region comprises two spaced segments (200,201) with respective segments (56,57) of the source. Two surface **channel** segments are on the upper surface of the inner parts of the segments (200,201) between their edges and the source segments. The external parts of the segments (200,201) which adjoin the source segment parts (56,57) remote from the **channel** segments have a higher conductivity than the neighbouring parts, so as to hinder switch-on of the parasitic bipolar transistors.
The drain region has two spaced segments (70), arranged spaced outside the segments of the main regions. A field-reduction surface region includes a first segment (71) arranged between a first segment (200) of the main region and the first segment (70) of the drain, also a second segment (71) between the second main-region segment and the second drain segment. The lateral component of current flow includes two paths under the two main segments.
ABEQ US 4866495 A UPAB: 19930923
A surface field redn. region disposed between drain and source regions extends from the chip surface and into its body and has a **charge** density of about 1 x 10 (raised to power 12) ions/cm square. A second surface field redn. region extends below the first region and the source and drain regions and has a **charge** density of from about 1.5 x 10 (raised to power 12) to 2.0 x 10 (raised to power 12) ions/cm square.
A substrate extends below the second region and is isolated from both drain and source regions to enable the use of the device as a high-**side** switch.
ADVANTAGE - No high electric field stress will appear in region near

edge of polysilicon gate, thus, no avalanche will occur in that very critical region.

ABEQ US 5023678 A UPAB: 19930923

The lateral conduction high power MOSFET chip has **integrated** control circuits for high-**side** switching applications. A surface field reduction region is disposed between drain and source regions extends from the chip surface and into its body and has a **charge** density of about 1x10 power12 ions/cm squared. A second surface field reduction region extends below the first region and the source and drain regions and has a **charge** density of from about 1.5x10 power12 to 2.0x10 power12 ions/cm squared.

A substrate extends below the second region and is isolated from both drain and source regions to enable the use of the device as a high-**side** switch.

USE - For high-**side** switch.

FS EPI

FA AB; GI

L101 ANSWER 7 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 1992-133853 [17] WPIX
DNN N1992-099883
TI Semiconductor device e.g. high electron mobility transistor - has potential well for channel-**free charge carriers**, formed between channel and substrate by heterojunction forming layer.
DC U12
IN BATTERSBY, S J
PA (PHIG) PHILIPS ELTRN UK LT; (PHIG) PHILIPS ELECTRONICS NV; (PHIG) PHILIPS ELECTRONICS UK LTD; (PHIG) PHILIPS ELTRN UK; (PHIG) PHILIPS GLOEILAMPENFAB NV; (PHIG) US PHILIPS CORP
CYC 5
PI EP 481555 A 19920422 (199217)* EN 12p
R: DE FR GB
GB 2248966 A 19920422 (199217) 25p
JP 04260339 A 19920916 (199244) 8p H01L021-338
US 5254863 A 19931019 (199343) 8p H01L029-80
EP 481555 B1 19960103 (199606) EN 13p H01L029-812
R: DE FR GB
DE 69116076 E 19960215 (199612) H01L029-812
AB EP 481555 A UPAB: 19931006
The transistor in a semiconductor substrate (2) includes a channel (10) between source (20) and drain (21) regions. The channel layer (11) forms a heterojunction (12) with a barrier layer (13) and has a **gate electrode** (25) above.

A potential well for the channel-**free charge carriers** is formed between the channel and substrate by a layer (31) forming heterojunctions with sandwiching barrier layers (33, 33'). The well is empty of free carriers for zero source-drain voltage, but is sufficiently deep and wide to trap hot carriers for high channel fields.

ADVANTAGE - Increased output impedance. (1/4)
1/4
ABEQ US 5254863 A UPAB: 19931207
The semiconductor device is formed by a semiconductor body (1) having a substrate (2) on which is provided a channel-defining region (10) extending between input and output regions (20) and (21). The channel-defining region (10) has a channel layer (11) forming a hetero-junction (12) with at least one barrier layer (13) to form within the channel layer a two-dimensional **free charge carrier** gas (14) of one conductivity type for providing a **conduction channel** controllable by a **gate electrode** (25). A potential well region (30) is provided between the substrate and the channel-defining region.

The potential well region has at least one potential well-defining layer (31) forming heterojunctions (32) with adjacent barrier layers (33) to define a potential well which is empty of **free charge carriers** of the one conductivity type when no voltage is applied between the input and output regions and which is sufficiently deep and wide to trap hot charge carriers of the one conductivity type which are emitted from the channel-defining region towards the substrate when a high lateral electrical field exists in the channel-defining region, thus constraining the hot charge carriers near to the **gate electrode** and enabling an improved output impedance when the device is an FET.

USE - As high electron mobility transistor.
Dwg.1/4
ABEQ EP 481555 B UPAB: 19960212
A semiconductor device comprising a semiconductor body (1) having a substrate (2) on which is provided a channel-defining region (10) extending between input and output regions (20 and 21), the channel-defining region (10) comprising a channel layer (11) forming a

heterojunction (12) with at least one barrier layer (13 1) so as to form within the channel layer (11) a two-dimensional **free charge carrier** gas (14) of one conductivity type for providing between the input and output regions (20 and 21) a **conduction channel** (14) controllable by a **gate electrode** (25) overlying the channel-defining region (10), a potential well region (30) being provided between the substrate (2) and the channel-defining region (10) which comprises at least one potential well-defining layer (31) forming heterojunctions (32) with adjacent barrier layers (33 1 and 33) to define for charge carriers of the one conductivity type a potential well (31) which is empty of **free charge carriers** of the one conductivity type when no voltage is applied between the input and output regions (20) and 21), the combined width of the potential well (31) and the spacing of the potential well (31) from the channel-defining region (10) being less than about a third of the length of the **gate electrode** (25) and the potential well (31) being sufficiently deep and wide to trap hot charge carriers of the one conductivity emitted from the channel-defining region (10) towards the substrate (2).
Dwg.1/4

FS EPI

L101 ANSWER 3 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 1998-132895 [13] WPIX
DNN N1998-105012 DNC C1998-043920
TI Fabrication of thin film transistors for liquid crystal displays - comprises back channel region separating source and drain regions, **doped** with **compensated** impurities to give high electric resistance.
DC L03 U11 U12 U14
IN NOGUCHI, K
PA (NIDE) NEC CORP; (NIDE) NIPPON ELECTRIC CO
CYC 21
PI EP 827210 A2 19980304 (199813)* EN 37p H01L029-786
R: AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
JP 10074946 A 19980317 (199821) 21p H01L029-786
KR 98019183 A 19980605 (199923) H01L029-772
US 6285041 B1 20010904 (200154) H01L029-04
KR 299555 B 20011215 (200249) H01L029-772
ADT EP 827210 A2 EP 1997-115034 19970829; JP 10074946 A JP 1996-228733 19960829; KR 98019183 A KR 1997-43170 19970829; US 6285041 B1 US 1997-921044 19970829; KR 299555 B KR 1997-43170 19970829
FDT KR 299555 B Previous Publ. KR 98019183
PRAI JP 1996-228733 19960829
IC ICM H01L029-04; H01L029-772; H01L029-786
ICS H01L021-336; H01L031-036; H01L031-0376; H01L031-20
AB EP 827210 A UPAB: 19980330
A thin film transistor comprises: (a) a substrate with a layered structure formed on it including; semiconductor with on its first **side** a gate insulating film and **gate electrode,** and on its second **side,** source and separated drain electrodes electrically connected to it; and (b) a back channel section between opposite ends of the source and drain electrodes including a high electric resistance part containing n- and p-type impurities, and located on the back of the semiconductor film with respect to an electrically **conductive channel**. Also claimed is the manufacture of the above transistor, by forming the layered structure and **doping** with impurities to form the high resistance part between the source and the drain region, on the semiconductor.

USE - Liquid crystal displays.

ADVANTAGE - The thin film transistor has a simple configuration and improved off characteristics.

Dwg.9/26

L79 ANSWER 43 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1987-265698 [38] WPIX
CR 1989-341718 [47]; 1993-093316 [11]; 1993-377445 [47]; 1994-048095 [06]; 1994-048096 [06]; 1996-299957 [30]; 1997-372071 [34]; 1998-494899 [42]
DNN N1987-199099
TI Producing multifunctional **region** semiconductor device - using mask-surrogate semiconductor process employing **dopant**-opaque **region** in wafer material for substrate structure.
DC P83 U11
IN HOLLINGER, T G
PA (ADPO-N) ADVANCED POWER TECHNOLOGY INC; (ADPO-N) ADVANCED POWER TECHNOLOGY INC
CYC 17
PI EP 238362 A 19870923 (198738)* EN 14p
R: AT BE CH DE ES FR GB GR IT LI LU NL SE
JP 62279677 A 19871204 (198803)
US 4748103 A 19880531 (198824) 14p
CA 1253262 A 19890425 (198921)
CA 1277437 C 19901204 (199103)
EP 238362 B1 19941228 (199505) EN 19p H01L021-24
R: AT BE CH DE ES FR GB GR IT LI LU NL SE
DE 3750909 G 19950209 (199511) H01L021-24
KR 9600387 B1 19960105 (199905) H01L029-78
ADT EP 238362 A EP 1987-302480 19870323; JP 62279677 A JP 1987-68747 19870323; US 4748103 A US 1986-842771 19860321; EP 238362 B1 EP 1987-302480 19870323; DE 3750909 G DE 1987-3750909 19870323, EP 1987-302480 19870323; KR 9600387 B1 KR 1987-2615 19870321
FDT DE 3750909 G Based on EP 238362
PRAI **US 1986-842771 19860321**
REP A3...8848; EP 148448; EP 148595; EP 70692; No-SR.Pub; US 4644637
IC G03C005-00; H01L021-24; H01L029-78
ICM H01L021-24; H01L029-78
ICS G03C005-00; H01L021-225
AB EP 238362 A UPAB: 19981021
A mask-surrogate pattern-definer is created having a defined outline in a multifunctional **region**. The unaltered outline per se of the pattern-definer is used as a control and self-alignment making agency to effect the making of the desired, final functional **regions** in the semiconductor device.

A base N-**doped** layer (18) and an N-**doped** **epitaxial** layer (20) are in the drain (14). A P-**doped** layer (22) forms the 'body' in the transistor (10). An N+ **doped** layer (24) forming the source in the transistor resides in the 'body' Immediately above these layers are a gate-oxide layer (Si02) (26) and two metallisation layers (28,30).

USE/ADVANTAGE - Reducing, practically to zero, likelihood of fatal defect occurring in final mfd. semiconductor device, even though entire usable area, i.e. as a single device, on a substrate, e.g. silicon wafer, may be occupied.
Dwg./17
ABEQ US 4748103 A UPAB: 19930922
The production method comprises the steps of forming over the oxide layer a **dopant** protective layer and creating a mask surrogate pattern-definer having a defined outline characteristic in the protective layer. The unaltered perimetral outline characteristic the only-created pattern-definer is employed for control and self-alignment masking to effect the making of the desired, final functional **regions** in the device, including a conductive-material deposition step.

The creating is accomplished in the absence of the use of any independent mask and is performed by laser.

ADVANTAGE - **Free** from mask-dependent failure.
ABEQ US 5182234 A UPAB: 19930922

A **dopant** opaque layer of polysilicon is deposited on gate oxide on the upper substrate surface to serve as a pattern definer during fabricatoin of the device. It provides control over successive P and N **doping** steps used to create the necessary operative junctions within a silicon substrate and the conductive structures formed on the substrate. A **trench** is formed in the upper silicon surface and a source conductive layer is deposited to electrically contact the source **region** as a gate conductive layer is deposited on the gate oxide layer. The **trench sidewall** is profile tailored using a O2-SF6 plasma etch technique. An oxide **sidewall** spacer is formed on the **sides** of the pattern definer and gate oxide structures, before depositing the conductive material. A planarising layer is applied and used as a mask for selectively removiny any conductive material deposited on the oxide spacer.

The polysilicon layer on the oxide is reduced in thickness during **trenching** so that any conductive material deposited on the spacers protrude upward for easy removal of excess, conductive material. The **sidewall** spacers can be sized, either alone or in combination with profile tailoring of the **trench**, to control source-**region** width (i.e. parasitic pinched base width) and proximity of the source conductor to the FET **channel**. Electrical contact between the source conductive layer and the source **regions** is enhanced by forming a low resistivity layer between them.

ADVANTAGE - Increased yield. (Dwg.13c/7

13c/7

ABEQ EP 238362 B UPAB: 19950207

A method, employing a mask-surrogate pattern definer, of producing a field-effect power MOS semiconductor device (10) in a substrate structure including a gate oxide layer (26) on an upper surface of a semiconductor substrate, the method being characterised by the following steps performed in the given order; forming a **dopant** protective layer (32) over the gate oxide layer (26); masking and patterning (34, 36) the **dopant** protective layer (32) by selectively removing a portion of the **dopant** protective layer to form a mask-surrogate pattern-definer (40) having a defined outline characteristic so that the pattern-definer protects an underlying gate oxide **region** (49) and a first portion of the upper surface of the substrate and to expose a second portion of the upper surface of the substrate within a **region** defined by the defined outline characteristic; performing a first **doping** step to introduce **dopant** (42) into said exposed second upper surface portion of the substrate so as to form a first MOS **region** (22), being a MOS body **region** of a first conductivity type, said first **region** extending by a lateral dimension (48) under a peripheral edge of the protective layer; performing a second **doping** step to introduce **dopant** (50) into said exposed second upper surface portion so as to form a second MOS **region** (24), being a MOS body **region** of a second conductivity type, opposite the first MOS **region** (22); said second **region** (24) being wholly contained in said first **region** (22) and extending to a distance within said dimension (48) along the upper surface of the substrate to define a MOS **channel** beneath said **region** (49) of the gate oxide layer (26); the **dopant** protective layer (32) being **dopant** opaque so as to prevent the introduced **dopants** (42, 50) from penetrating the underlying gate oxide **region** (49); simultaneously etching the **dopant** protective layer and the expose upper surface of the substrate after the first and second **doping** steps to form a **trench** (60) in the exposed upper surface portion of the substrate, the **trench** being formed to a **trench** depth greater than the depth (52) of the second **region** but less than the depth (46) of the first **region** (22), and formed of a width less than that of the second **region** (24) such that separated **regions**

(24') of the second conductivity type are provided at **sidewalls**
of the **trench,** the separated **regions** (24')
constituting source **regions** of the MOS semiconductor device
(10); and depositing a layer of conductive material over the entire upper
surface of the device to form simultaneousl

L79 ANSWER 45 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1987-151744 [22] WPIX
DNN N1987-113829
TI Lateral insulated gate transistor - has additional heavily **doped** **region** near base **region** to improve latch-up immunity.
DC U12
IN ADLER, M S; PATTANAYAK, D N
PA (GENE) GENERAL ELECTRIC CO
CYC 4
PI EP 224269 A 19870603 (198722)* EN 49p
R: DE NL
JP 62189758 A 19870819 (198739)
US 4963951 A 19901016 (199044)
EP 224269 B1 19921014 (199242) EN 21p H01L029-72
R: DE NL
DE 3686971 G 19921119 (199248) H01L029-72
ADT EP 224269 A EP 1986-116513 19861127; JP 62189758 A JP 1986-278905 19861125; US 4963951 A US 1985-803049 19851129; EP 224269 B1 EP 1986-116513 19861127; DE 3686971 G DE 1986-3686971 19861127, EP 1986-116513 19861127
FDT DE 3686971 G Based on EP 224269
PRAI **US 1985-803049 19851129**
REP 3.Jnl.Ref; A3...8908; EP 111803; GB 1400574; GB 2156151; No-SR.Pub; 03Jnl.Ref
IC ICM H01L029-72
ICS H01L027-02; H01L029-10
AB EP 224269 A UPAB: 19930922
The transistor includes an anode **terminal** (22), an anode contact (20), a P+ anode **region** (18), a lightly **doped** N buffer **region** (16), an N drift **region** (14), a P base **region** (28), and N+ source **region** (30), a cathode contact (32) and a cathode **terminal** (34).

The lateral insulated gate transistor is disposed not on a P-substrate (12) alone but on the P+ substrate with an **epitaxially** disposed P- layer. The P+ substrate provides a drain or sink for holes or minority **carriers**, contributing to the collector current of the vertical transistor.

ADVANTAGE - Improved current capacity and immunity to latch-up.
3/12
ABEQ DE 3686971 G UPAB: 19930922
The transistor includes an anode **terminal** (22), an anode contact (20), a P+ anode **region** (18), a lightly **doped** N buffer **region** (16), an N drift **region** (14), a P base **region** (28), and N+ source **region** (30), a cathode contact (32) and a cathode **terminal** (34).

The lateral insulated gate transistor is disposed not on a P-substrate (12) alone but on the P+ substrate with an **epitaxially** disposed P- layer. The P+ substrate provides a drain or sink for holes or minority **carriers**, contributing to the collector current of the vertical transistor.

ADVANTAGE - Improved current capacity and immunity to latch-up.
ABEQ EP 224269 B UPAB: 19930922
A lateral insulated gate bipolar transistor having a substantially planar upper surface comprising: a substrate (60) on one type (P+) conductivity; a first layer (12) of said one type conductivity (P-) disposed contiguous to said substrate the substrate (60) being more heavily **doped** than the first layer (12); a second layer (14) of an opposite type conductivity (N) disposed contiguous to said first layer and forming a portion of said upper surface of said device; a first **region** (16) of said opposite type conductivity (N) disposed within said second layer and forming a portion of said upper surface of said device; a second **region** (18) of said one type conductivity (P) disposd in said

first **region,** spaced from said second layer (14) and forming a portion of said upper surface; a third **region** (28) of said one type conductivity (P) disposed within said second layer (14), spaced from said first **region,** forming a portion of said upper surface and having a basic **doping** concentration; a fourth **region** (30) of said opposite type (N) conductivity disposed in said third **region** (28), forming a portion of said upper surface, spaced from said second layer (14) to define a **channel** portion of said third **region** (28) adjacent said upper surface between said fourth **region** (30) and said second layer (14) at the **side** of said fourth **region** (30) toward said second **region;** an insulation layer (36) disposed on said upper surface of said device and covering a portion of said third (28) and fourth **regions** (30) including said **channel** portion of said third **region;** a gate electrode (38) covering a portion of said insulation layer and aligned over at least said **channel** portion of said third **region** (28) and responsive to an appropriate bias for inducing a **channel** in said **channel** portion of said third **region** coupling said second layer to said fourth **region;** a power electrode (32) in contact with portions of said third (28) and fourth (30) **regions** which are spaced from said **channel** portion of said third **region** and shorting said third **region** (28) to said fourth **region** (30) to inhibit inadvertent forward biasing of the junction between said third and fourth **regions;** and additional one type conductivity (P) determining **dopant** disposed in the vicinity of said third **region** (28), said additional **dopant** establishing a buried **region** (66) for increasing the conductivity for **carriers** of said one type conductivity (P) in the vicinity of said third **region** (28) away from said junction between said third (28) and fourth (30) **regions** to above that provided by said basic **doping** concentration of said third **region** (28) to establish a current path for said **carriers** of said one type conductivity (P) away from the portion of said third **region** (28) which is adjacent to the portion of said junction along the surface of said fourth **region** (30) which is remote from said upper surface; wherein said buried **region** (66) of said one type conductivity (P) extends from said upper surface into the first layer (12) and in major portion is adjacent and underlies a portion of said third **region** (28) directly be
1/10

ABEQ US 4963951 A UPAB: 19930922

The lateral insulated gate transistor (10) has a lightly **doped** P substrate (12) having a N type layer (14) **epitaxially** disposed thereon. An N type buffer **region** (16) is disposed in the layer, and a P+ anode **region** (18) is disposed within the N buffer **region.** A metallized contact (20) is applied to the P+ anode **region** and a **terminal** (22) is electrically connected to the metallized layer. On the cathode **side** of the device, a P base **region** 28 is disposed in the **epitaxial** layer and an N+ cathode **region** (30) is disposed within the P base.

A metal contact 32 is disposed over and in contact with the N+ cathode **region** and the P base **region** and serves as an electrical contact for each **region** and additionally shorts the source **region** to the base **region.** A **terminal** 34 is applied to the cathode contact. The cathode portion of the device is separated from the anode portion of the device by a portion of the **epitaxial** layer which is designated as the N- drift layer. The surface of the device is formed by a portion of the **epitaxial** layer, the anode **region** the buffer **region** 16, the base **region** 28 and source **region** 30.

ADVANTAGE - Has improved immunity to latch up. @@

L79 ANSWER 48 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1985-242677 [39] WPIX
DNN N1985-181535
TI Bidirectional power FET with substrate referenced shield - has steering-diode function for referencing shielding electrode performed by junctions present in **integrated** structure.
DC U12
IN BENJAMIN, J A; LADE, R W; SCHUTTEN, H P
PA (EAYT) EATON CORP
CYC 6
PI US 4541001 A 19850910 (198539)* 11p
EP 205639 A 19861230 (198652) EN
R: DE FR GB NL
JP 62032649 A 19870212 (198712)
ADT US 4541001 A US 1982-421933 19820923; EP 205639 A EP 1985-107809 19850625; JP 62032649 A JP 1985-168460 19850730
PRAI **US 1982-421933 19820923**
IC H01L029-78
AB US 4541001 A UPAB: 19930925
A shielding electrode is insulated between two electrodes in a notch between laterally spaced source and **channel** regions joined by a common drift region around the bottom of the notch. The shielding electrode is ohmically connected to the substrate containing the common drift region to be at the same potential level and within a single junction drop of a respective main electrode across the junction between the respective **channel** containing region and drift region.

The steering diode function for referencing the shielding electrode is performed by junctions already present in the **integrated** structure. The shielding electrode prevents the electric field gradient toward the gate electrode on one **side** of the notch from inducing depletion in the drift region along the opposite **side** of the notch.

ADVANTAGE - Prevents unwanted inducement of conduction **channels** in drift region during the OFF state, no need for discrete dedicated steering diodes, high off state voltage blocking capacity.
1/8
FS EPI
FA AB

L79 ANSWER 57 OF 64 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:824564 HCAPLUS
DN 133:368475
TI Silicon carbide power devices having **trench**-based silicon carbide **charge** coupling **regions** therein
IN Baliga, Bantval Jayant
PA North Carolina State University, USA
SO PCT Int. Appl., 47 pp.
CODEN: PIXXD2
DT Patent
LA English
IC ICM H01L029-24
ICS H01L029-06; H01L029-872; H01L029-78; H01L029-808
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2000070684	A2	20001123	WO 2000-US13455	20000516 <--
	WO 2000070684	A3	20010614		
	W: AE, AL, AM, AT, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU,				
	US 6313482	B1	20011106	US 1999-312980	19990517
PRAI	US 1999-312980	A	19990517 <--		

AB Si carbide power devices having **trench**-based **charge** coupling **regions** include a Si carbide substrate having a Si carbide drift **region** of 1st cond. type (e.g., N-type) and a **trench** therein at a 1st face thereof. A uniformly **doped** Si carbide **charge** coupling **region** of 2nd cond. type (e.g., an in-situ **doped epitaxial** P-type **region**) is also provided in the **trench**. This **charge** coupling **region** forms a P-N rectifying junction with the drift **region** that extends along a **sidewall** of the **trench**. The drift **region** and **charge** coupling **region** are both uniformly **doped** at equiv. and relatively high net majority **carrier doping** concns. (e.g., 1 .times. 1017 cm-3) so that both the drift **region** and **charge** coupling **region** can be depleted substantially uniformly when blocking reverse voltages. This combination of preferred drift and **charge** coupling **regions** improves the elec. field profile in the drift **region** to such an extent that very low forward on-state drift **region** resistance can be achieved simultaneously with very high reverse blocking voltage capability. Si carbide switching devices that can advantageously use the preferred combination of drift and **charge** coupling **regions** include Schottky barrier rectifiers (SBRs), junction field effect transistors (JFETs) and metal-oxide-semiconductor field effect transistors (MOSFETs).

L79 ANSWER 49 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1985-147883 [25] WPIX
DNN N1985-111578
TI Hybrid power switching semiconductor - combines IGFET and MOSFET with coupled gates to combine low loss with potential high speed operation.
DC U12
IN BALIGA, B J; BALIGA, B
PA (GENE) GENERAL ELECTRIC CO
CYC 5
PI EP 144909 A 19850619 (198525)* EN 28p
R: DE FR NL
JP 60191518 A 19850930 (198545)
US 4618872 A 19861021 (198645)
EP 144909 B1 19920722 (199230) EN 15p H01L027-06
R: DE FR NL
DE 3485831 G 19920827 (199236) H01L027-06
ADT EP 144909 A EP 1984-114414 19841128; JP 60191518 A JP 1984-255857 19841205; US 4618872 A US 1983-558403 19831205; EP 144909 B1 EP 1984-114414 19841128; DE 3485831 G DE 1984-3485831 19841128, EP 1984-114414 19841128
FDT DE 3485831 G Based on EP 144909
PRAI **US 1983-558403 19831205**
REP A3...8721; DE 3147075; EP 118007; FR 2524710; No-SR.Pub
IC ICM H01L027-06
ICS H01L023-52; H01L029-78; H03K017-68
AB EP 144909 A UPAB: 19930925
An **integrated** power switching semiconductor device (10) comprising; a body comprising; a body (16) of semiconductor material including an insulated-gate transistor part (12) and an insulated-gate field-effect transistor part (14), said body having first and second opposed principal surfaces (18, 20) on opposite **sides** thereof; a first base layer (22) of one conductivity type common to both said insulated-gate transistor part and said insulated-gate field-effect transistor part; a first main **terminal** region (28) adjacent said first base layer and extending to said first principal surface (18) said first main **terminal** region including at least a zone (34) heavily-doped to a conductivity type opposite to the conductivity type of said one conductivity and defining a PN junction (32) with said first base layer (22) within said insualted gate transistor part (22) within said insulated gate transistor part (12), and said first base layer and said first main **terminal** region including a buried layer (36) heavily doped to the first conductivity for avoiding bipolar conduction within said insulated-gate field-effect transistor part (14) a second base region (45) of the opposite conductivity type and having two separated portions (46, 48) embedded in said first base layer (22), one of said portions (46) of said second base region being included in said insulated-gate transistor part (12) and the other of said portions (48) of said second base region being included in said insulated-gate field-effect transistor part (14); a first region (50) of the one conductivity type being included in said insulated-gate transistor part (12) embedded in said one portion (46) of said second base region (45); a second region (52) of the one conductivity type included in said insulated-gate field effect transistor part (14) embedded in said other portion (48) of said second base region (45); a **terminal** electrode overlying at least partly said second base region (45) and said first and second region (50) and being in contact therewith; a first **channel** region (54) included in said insulated-gate transistor portion (46) within said second base region (45) of the opposite conductivity type, and a second **channel** region (56) included in said insulated-gate field-effect transistor portion (48) within said second base region (45) of the opposite conductivity type, said first and second regions (50, 52) of the one conductivity type being spaced from the respective portions of said first base layer to define the

extent of the respective **channel** regions therebetween, first and second gate electrodes (70, 72) respectively disposed over said first and second **channel** regions (54, 56) and insulatingly spaced therefrom, said gate electrodes configured for inducing, when gate voltage is applied thereto, respective conduction paths of the one conductivity type in the respective **channel** regions beneath the respective energized gate electrodes; a resistance element (RG) connected between said firt
2/6

ABEQ DE 3485831 G UPAB: 19930925
The insulated gate transistor (IGT) and MOSFET portions of the device include gate structures each having an associated gate electrode capacitance. A resistance element connects these gates. The gate structures pref. comprise polysilicon electrodes, and the resistance element comprises a polysilicon bridge formed at the same time during manufacture.

The device has only a simple gate **terminal** which is connected relatively directly to one of the two gates, and via the resistance to the other gate. An R.C. time delay network is thus formed. Two different types of power switching functions are achieved depending on which gate is most directly connected.

ADVANTAGE - Has long steady state and switching losses.

ABEQ EP 144909 B UPAB: 19930925
An **integrated** power swtiching semiconductor device (10) comprising; a body comprising; a body (16) of semiconductor material including an insulated-gate transistor part (12) and an insulated-gate field-effect transistor part (14), said body having first and second opposed principal surfaces (18, 20) on opposite **sides** thereof; a first base layer (22) of one conductivity type common to both said insulated-gate transistor part and said insulated-gate field-effect transistor part; a first main **terminal** region (28) adjacent said first base layer and extending to said first principal surface (18) said first main **terminal** region including at least a zone (34) heavily-doped to a conductivity type opposite to the conductivity type of said one conductivity and defining a PN junction (32) with said first base layer (22) within said insualted gate transistor part (22) within said insulated gate transistor part (12), and said first base layer and said first main **terminal** region including a buried layer (36) heavily doped to the first conductivity for avoiding bipolar conduction within said insulated-gate field-effect transistor part (14) a second base region (45) of the opposite conductivity type and having two separated portions (46, 48) embedded in said first base layer (22), one of said portions (46) of said second base region being included in said insulated-gate transistor part (12) and the other of said portions (48) of said second base region being included in said insulated-gate field-effect transistor part (14); a first region (50) of the one conductivity type being included in said insulated-gate transistor part (12) embedded in said one portion (46) of said second base region (45); a second region (52) of the one conductivity type included in said insulated-gate field effect transistor part (14) embedded in said other portion (48) of said second base region (45); a **terminal** electrode overlying at least partly said second base region (45) and said first and second region (50) and being in contact therewith; a first **channel** region (54) included in said insulated-gate transistor portion (46) within said second base region (45) of the opposite conductivity type, and a second **channel** region (56) included in said insulated-gate field-effect transistor portion (48) within said second base region (45) of the opposite conductivity type, said first and second regions (50, 52) of the one conductivity type being spaced from the respective portions of said first base layer to define the extent of the respective **channel** regions therebetween, first and second gate electrodes (70, 72) respectively disposed over said first and second **channel** regions (54, 56) and insulatingly spaced

therefrom, said gate electrodes configured for inducing, when gate voltage is applied thereto, respective conduction paths of the one conductivity type in the respective **channel** regions beneath the respective energized gate electrodes; a resistance element (RG) connected between said firt and second gate electrodes (70, 72); and a device gate conductor (G1; G2) connected directly t
1/6

ABEQ US 4618872 A UPAB: 19930925

The hybrid power switches **integrate** IGT and MOSFET structures. The IGT and MOSFET portions include respective gate structures each having an associated gate electrode capacitance. A resistance element connects the IGT and MOSFET gates. The gate structures comprise polysilicon electrodes, and the resistance element comprises a polysilicon bridge formed at the same time during device fabrication.

The overall device has only a single gate **terminal,** which is connected relatively directly to one of the IGT and MOSFET gates, and indirectly through the resistance element to the other of the IGT and MOSFET gates such that an RC time delay network is defined. Two different types of power switching functions are achieved depending upon whether the overall device gate **terminal** is connected nearer the IGT gate or the MOSFET gate.

ADVANTAGE - Eliminates current tailing.

FS EPI

FA AB

L79 ANSWER 51 OF 64 WPIX (C) 2002 THOMSON DERWENT
AN 1982-52604E [26] WPIX
TI Controllable semiconductor module - with insulated gate of V-notch underlain by P-type **channel**.
DC L03 U12
PA (ZFTM) VEB ZFT MIKROELEKTRONIK FORSCH TECH; (WAGN-I) WAGNER S
CYC 5
PI DE 3131608 A 19820624 (198226)* 23p
DD 154049 A 19820217 (198230)
JP 57103353 A 19820626 (198231)
DD 154049 B 19830223 (198325)
CS 8106263 A 19841119 (198505)
US 4550332 A 19851029 (198546)
ADT US 4550332 A US 1981-319369 19811109
PRAI **DD 1980-224827 19801030**
IC H01L029-74
AB DE 3131608 A UPAB: 19930915
A semiconductor module which can be controlled by a small power input like a thyristor, for use as a link between data processing micro-electronic circuits and in telephone systems, has a V- or U-shaped notch between two electrodes, covered by an insulated gate. A **channel** area, pref. of the p-type, lies below the deepest part of the notch and is joined by an n-type substrate. The latter joins one **side** of the notch to an electrode region underlying one electrode; the other **side** of the notch is bridged by another electrode region to the other electrode.
This new module requires no special extinction circuit to cut the module OFF.
1
ABEQ US 4550332 A UPAB: 19930915
Gate controlled semiconductor device has a semiconductor substrate with a V- or U-shaped recess (4) protruding from the top surface. An insulating layer (3) covers the recess followed by a conducting layer for forming a gate (6). A second insulating layer covers the surface of the substrate and an ohmic contact in at an opening at one **side** relative to the gate. An electrode (5) is connected to the ohmic contact which is connected to a semi conductor region (8) which has a larger concn. of majority **carriers** than the substrate.
There is a second ohmic contact at an opening on the other **side** of the gate and an electrode (7) is connectedn to it. Another semiconductor region (10) of relative large **carrier** concn. is adjacent to the second contact and the substrate extends to the opposite **side** of the recess. A **channel** (9) of second conductivity, in the absence of electrical fields, is adjacent to and below the tip of the recess, the first semiconductor region, and part of the first contact.
USE/ADVANTAGE - Power control circuits in which the device can be controlled by its gate without power consumption.
FS CPI EPI
FA AB

L79 ANSWER 54 OF 64 JAPIO COPYRIGHT 2002 JPO
AN 1993-160407 JAPIO
TI VERTICAL INSULATING GATE TYPE SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF
IN TOKURA NORIHITO; OKABE NAOTO
PA NIPPONDENSO CO LTD
PI JP 05160407 A 19930625 Heisei
AI JP 1991-324734 (JP03324734 Heisei) 19911209
PRAI **JP 1991-324734** 19911209
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1993
IC ICM H01L029-784
AB PURPOSE: To provide a power element of double diffusion structure, in which ON resistance can be lowered and also threshold voltage and the resistance value inside a pinch layer can be set independently.
CONSTITUTION: Arsenic is diffused into the outermost surface of an n<SP>-</SP>-type epitaxial layer 2 so as to form a gate oxide film 3 and a gate electrode 4, and then, by DSA technology and double diffusion, a p-type base region 8 and an n<SP>+</SP>-type source layer 7 are formed in alignment with the gate electrode 4. Hereby, at the outermost surface, the junction depth in the lateral direction of the p-type base region 8 is **compensated**, and substantially the length of a channel 9 becomes short. Moreover, in case of designing it with the same threshold voltage as conventional, the density of the impurities of the p-type base region 8 can be higher by the amount of impurity density of the arsenic at the outermost surface than conventional, so the resistance value of the p-type pinch layer 14 made right below the n<SP>+</SP>-type source layer 7 in the p-type base region 8 can be lowered by that amount.

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L79  ANSWER 60 OF 64  HCAPLUS  COPYRIGHT 2002 ACS
AN   2000:278204  HCAPLUS
DN   132:287492
TI   Semiconductor power component, operational method, and use thereof as a
     switch
IN   Schlogl, Andreas; Schulze, Hans-joachim; Deboy, Gerald
PA   Siemens A.-G., Germany
SO   PCT Int. Appl., 25 pp.
     CODEN: PIXXD2
DT   Patent
LA   German
IC   ICM  H01L029-78
     ICS  H01L029-808; H01L029-08; H01L023-44; H02J015-00
CC   76-3 (Electric Phenomena)
FAN.CNT 1
     PATENT NO.       KIND  DATE           APPLICATION NO.  DATE
     ---------------  ----  --------       ---------------  --------
PI   WO 2000024061     A1   20000427       WO 1999-DE3318   19991015 <--
         W:  JP, KR, US
         RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL,
             PT, SE
PRAI DE 1998-19847820       19981016  <--
AB   A compensating component is cooled to a temp. of below 250 K,
     preferably to temps. below 80 K and preferably, liq. N2 is used.  This
     enables components with particularly good operating characteristics to be
     obtained.
ST   semiconductor power component switch cooling liq nitrogen MOSFET diode;
     compensating power component cooling thyristor semiconductor
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L101 ANSWER 1 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 2001-041408 [05] WPIX
DNN N2001-030880 DNC C2001-012066
TI Gate for semiconductor transistor device with highly doped central portion compared with sides, with work function of sides varying relative to central portion.
DC L03 U11
IN PONOMAREV, Y; STOLK, P A
PA (PHIG) KONINK PHILIPS ELECTRONICS NV
CYC 27
PI WO 2000077828 A2 20001221 (200105)* EN 25p H01L000-00
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: JP KR
EP 1138058 A2 20011004 (200158) EN H01L021-00
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
KR 2001072403 A 20010731 (200209) H01L021-336
PRAI EP 1999-201869 19990611
AB WO 200077828 A UPAB: 20010124

NOVELTY - An active region (4) is defined with a channel (13) between source (11,9) and drain (12,9). A dielectric (14) is applied which has a recess at the area where the gate will be. An insulator layer is applied in the recess and the gate dielectric (17) is provided. Two conductive layers which form the gate (22) are applied with the first being thin compared to the width of the recess and fill the recess in the dielectric.

DETAILED DESCRIPTION - Manufacture of semiconductor device having active region of first conductivity type with transistor and gate insulated from channel at surface of the semiconductor body (1). The channel extends between source and drain zone of second conductivity type and the sides (19) of the channel are in contact with the side of gate dielectric. The gate dielectric and channel establish a work function of the gate which varies along the length of the channel. After definition of the active region, a dielectric is applied which has a recess at the area where the gate will be. An insulator layer is applied in the recess and the gate dielectric is provided. Two conductive layers which form the gate are applied with the first being thin compared to the width of the recess and fill the recess in the dielectric.

USE - Manufacture of semiconductor device.

ADVANTAGE - The length of the gate produced can be shorter than previous methods and can even be approximately the size of the minimum feature size obtainable by lithography. The work function of the sides of the gate vary relative to the work function of the central portion. This **compensates** for threshold voltage reduction due to short channel effects (claimed).

DESCRIPTION OF DRAWING(S) - The figure shows a cross section of the device comprising a transistor.

Semiconductor body 1
Active region 4
Extended source 11,9
Extended drain 12,9
Channel 13
Dielectric 14
Gate dielectric 17
Side portions 19
Central portion 21
Gate 22
Dwg.15/15

TECH WO 200077828 A2UPTX: 20010124

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Process: Prior to application of the dielectric, a patterned layer is applied at the area of the planned gate. Source and drain are formed in the semiconductor body using the patterned layer as a mask. Thickness of the dielectric layer is

greater than thickness of the patterned layer and the patterned layer is exposed by removing part of the thickness of the dielectric. The patterned layer is then removed to leave a recess in the dielectric.
Preferred Gate: A layer of the first conductivity type material is implanted with impurities of the second conductivity type perpendicular to the surface to produce a heavily doped central region (21) and lighter **doped sides** (19).
Preferred Transistor: The transistor is applied as an n-channel transistor and another is applied as a p-channel transistor. Both are fabricated using one common first conductive layer.

FS CPI EPI

L101 ANSWER 25 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:173050 HCAPLUS
DN 122:93517
TI Evolution of a **doping** zone with a low temperature field effect in weakly **compensated** silicon with a high level of **doping**
AU Vedeneev, A. S.; Gaivoronskii, A. G.; Zhdan, A. G.; Modelli, A.; Ryl'kov, V. V.; Tkach, Yu. Ya.
CS Inst. Radiotekh. Elektron., Ryazino, 141120, Russia
SO Pis'ma v Zhurnal Eksperimental'noi i Teoreticheskoi Fiziki (1994), 60(5-6), 457-61
CODEN: PZETAB; ISSN: 0370-274X
PB Nauka
DT Journal
LA Russian
CC 76-1 (Electric Phenomena)
AB At a low-temp. field effect in Si:B, contg. 1017-18 cm-3 B, the the **cond. channels** at surface form at relatively high electrode potentials depending on **doping** degree. At a hole depletion of Si surface the fluctuating potential forms due to impurity recharging and at a hole enrichment due to occupation of the upper Hubbard band in the conditions of hole-gas quantization.
ST **doping** zone evolution silicon boron **dopant**;

L101 ANSWER 13 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 1984-140822 [23] WPIX
DNN N1984-104481 DNC C1984-059489
TI **Lateral** auto-**doping compensation** - by diffusing **dopants** of opposite type from substrate.
DC L03 U11
IN FISCHER, A; KUEHNE, H; MUELLER, B; RICHTER, F; SPERLING, R
PA (DEAK) AKAD.WISSENSCHAFTEN DDR
CYC 1
PI DD 206799 A 19840208 (198423)* 12p
ADT DD 206799 A DD 1981-235126 19811126
PRAI DD 1981-235126 19811126
IC C30B025-02
AB DD 206799 A UPAB: 19930925

Lateral autodoping in CVD epitaxial layers is **compensated** by producing in the substrate between the high-impurity areas a buried layer of **dopants** of the opposite type by ion implantation. In the initial phase of the following epitaxial growth the buried **dopants** do not penetrate the substrate surface much but they migrate during the high-temp. load deep enough to interrupt the more **conductive channel** between adjoining high-impurity areas.

This **compensates** the **lateral** autodoping which causes an intensified galvanic coupling of adjoining buried low-resistance areas.

0/4
FS CPI EPI
FA AB

L101 ANSWER 27 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:571178 HCAPLUS
DN 119:171178
TI Sub-.mu.m wide channels with surface potential **compensated** by focused silicon ion beam implantation
AU Fujisawa, Toshimasa; Saku, Tadashi; Hirayama, Yoshiro; Tarucha, Seigo
CS Basic Res. Lab., NTT, Musashino, 180, Japan
SO Appl. Phys. Lett. (1993), 63(1), 51-3
CODEN: APPLAB; ISSN: 0003-6951
DT Journal
LA English
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 71
AB The authors propose and demonstrate a novel technique using focused Si ion beam implantation to produce high-quality mesoscopic channels. Low-energy Si implantation **compensates** the surface potential of a modulation-**doped** heterostructure that is designed to have no **conductive channels** at the heterointerface. The implantation forms a **conductive channel** sepd. from the damaged implanted region. The mobility of the channel is improved by decreasing the ion energy at 100-35 keV. Sub-.mu.m to 5 .mu.m wide channels fabricated by 35 keV Si+ ions show a mobility of 5.3 .times. 105 cm2/V s and a ballistic length of 3.1 .mu.m at 1.5 K.

L101 ANSWER 28 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:437685 HCAPLUS
DN 117:37685
TI Grain boundary electrostatic potential as a function of acceptor and donor doping in titania
AU Ikeda, Jeri Ann S.; Chiang, Yet Ming; Madras, Cynthia G.
CS Dep. Mater. Sci. Eng., Massachusetts Inst. Technol., Cambridge, MA, USA
SO Ceram. Trans. (1991), 24(Point Defects Relat. Prop. Ceram.), 341-8
CODEN: CETREW; ISSN: 1042-1122
DT Journal
LA English
CC 76-2 (Electric Phenomena)
AB Observation of the grain boundary solute segregation and depletion in TiO2 co-doped with the acceptor Al and the donor Nb, indicates that the electrostatic potential can be titrated in sign and magnitude by varying lattice defect structure and temp. An isoelec. line (zero potential) lying to the slightly donor-**doped side** at 1200-1550.degree. was established. Quantification of the excess charge d. in the space charge layer by STEM leads to the detn. of the boundary potential. For donor-doped samples in the vacancy **compensated** regime, the formation energy of the Ti vacancy can be obtained using these values of the boundary potential.
ST grain boundary electrostatic potential titania; aluminum doping titania; niobium doping titania; space charge doping titania
IT Space charge
(of grain boundaries in doped titania)

L101 ANSWER 30 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 1974:8291 HCAPLUS
DN 80:8291
TI MOS [metal oxide semiconductor] threshold shifting by ion implantation
AU Sigmon, Thomas W.; Swanson, Richard
CS Hewlett-Packard Lab., Palo Alto, Calif., USA
SO Solid-State Electron. (1973), 16(11), 1217-32
CODEN: SSELA5
DT Journal
LA English
CC 71-13 (Electric Phenomena)
AB A theor. description of threshold shifting of MOS devices by implantation of an impurity beneath the control electrode is presented. Exptl. measurements are presented which verify the theor. predictions. In particular, MOS capacitors and transistors were used to verify exptl. the theory (n-type Si substrates to verify the case of p-channel devices). Implanted layers sufficient to **compensate** the background substrate **doping** were used. This layer creates a buried **conducting channel** beneath the gate that is isolated from the substrate by the p-n junction. Modulation of this conduction region by the surface depletion region was responsible for the transistor action. For n-type substrates (p-channel devices) ion energies of 33 and 53 keV were selected for use with gate oxides of .apprx.0.1 .mu.m. B doses ranged from 5 .times. 1010 to 2 .times. 1012 atoms/cm2. threshold shifts from 0.2 to 5 V were obsd. Device performance was not degraded by the implantation. Annealing temps. .gtoreq. 500.degree. were sufficient to anneal the damage caused by the implantation. Changes in the characteristic C vs. V (capacitance vs. voltage) curves of the devices were predicted and exptl. obsd. A method of picking the approx. turn-off voltage of the devices from the C vs. V curves is pointed out.
ST semiconductor device threshold shifting; ion implantation semiconductor

L101 ANSWER 12 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 1984-172445 [28] WPIX
DNN N1984-128541
TI D-A converter with substrate bias voltage **compensation** - has resistance branch point supplied with two voltage levels via respective resistors according to MSB value.
AW SIGNIFICANT BIT.
DC U13 U21
IN HINO, Y
PA (FUIT) FUJITSU LTD
CYC 5
PI EP 113216 A 19840711 (198428)* EN 26p
R: DE FR GB
JP 59125121 A 19840719 (198435)
US 4713649 A 19871215 (198806)
EP 113216 B 19890712 (198928) EN
R: DE FR GB
DE 3380197 G 19890817 (198934)
ADT EP 113216 A EP 1983-307559 19831213; JP 59125121 A JP 1982-233909 19821229; US 4713649 A US 1986-847093 19860402
PRAI JP 1982-233909 19821229
REP 1.Jnl.Ref; A3...8634; FR 2288424; No-SR.Pub; US 3541354; US 3832707; EP 26579; EP 28695
IC H03K013-05; H03M001-66
AB EP 113216 A UPAB: 19930925
The converter includes a resistance network having at least one resistor connected between an output terminal of an inverter and a terminating resistor. The output terminal and the (each) connecting point between the resistors constituting respective branch points of the network. A number of switching circuits are provided, connected to respective branch points and supplying them with two voltage levels according to values, 1 or 0, of respective bits of a digital signal input to the converter.

At least one switching circuit has a configuration including two further resistors and operable so that the branch point connected to the associated switching circuit is supplied with one voltage level via one resistor and the other level via the other resistor. Pref. the inverter comprises a pair of CMOS transistors, with further n- and p- MOS transistors for each switching circuit.

ADVANTAGES - Has improved input-output signal characteristic linearity and reduced output distortion.
6/7
ABEQ EP 113216 B UPAB: 19930925
An integrated circuit digital-analog converter, formed on a substrate which, when the integrated circuit is in operation, receives a substrate bias voltage, the converter comprising a resistance network comprising resistors (R, 2R) constituted by p or n-type conductive semiconductor channels embedded in semiconductor material of opposite conductivity type, with at least one first resistor (R) connected, connected in series when more than one first resistor (R) is provided, between an output terminal (Vout) of the converter and a second, terminating, resistor (2R), the output terminal (Vout) and the or each connecting point between those resistors constituting respective branch points of the network, a plurality of switching circuits (IO to In), connected to respective branch points, operable to supply respective branch points from a first supply voltage level (VREF), or from a second supply voltage level, in dependence upon the values (1 or 0) of respective bits (AO to An) of a digital signal input to the converter, characterised in that at least one of the switching circuits (10) has a configuration including third (2R') and fourth (2R") resistors, also constituted by p or n-type **conductive channels** embedded in semiconductor material of opposite conductivity type, and operable such that the branch point (Vout, O') connected to the switching circuit (IO) concerned is supplied from the

first supply voltage level (VREF) through the third resistor (2R') and is supplied from the second supply voltage level through the fourth resistor (2R") and wherein the nominal resistance of the or each third resistor (2R') differs slightly from the nominal resistance of the or each fourth resistor (2R") thereby to **compensate** for the effect of substrate bias voltage on the resistances of the resistors, when the integrated circuit is in operation, both those nominal resistances being close to twice the resistance of the or each first resistor (R), and the terminating resistor (2R) hav

ABEQ US 4713649 A UPAB: 19930925

The converter comprises a ladder circuit resistance network and switching device comprising p-channel and n-channel MOS transistors. The distortion of analog signals generated by non-linear characteristics of resistors fabricated using p-channel or n-channel materials in the semiconductor are improved by replacing an inverter element module of the ladder circuit with T-type inverter circuit element module, and adjusting the resistance value of both the **side** branches of the T-type circuit.

ADVANTAGE - Has improved linearity in analogue output signal as compared to digital input signal.

FS EPI

L101 ANSWER 10 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 1985-117647 [20] WPIX
DNN N1985-088515
TI IGFET push-pull digital signal switching circuit - keeps **gate electrode** of non-conducting transistor at voltage level equal to or lower than threshold using temp. **compensated** circuit.
DC U13 U21
PA (PHIG) PHILIPS GLOEILAMPENFAB NV; (PHIG) PHILIPS GLOEILAMPEN NV
CYC 9
PI EP 141474 A 19850515 (198520)* EN 11p
R: DE FR GB IT
NL 8303835 A 19850603 (198527)
JP 60174519 A 19850907 (198542)
CA 1212427 A 19861007 (198645)
US 4642485 A 19870210 (198708)
EP 141474 B 19900207 (199006) EN
R: DE FR GB IT
DE 3481363 G 19900315 (199012)
KR 9209201 B1 19921014 (199412) H03K017-00
AB EP 141474 A UPAB: 19930925
A transistor (T5) is connected as a diode and via two cross-coupled transistors (T6,T7) to the **gate electrodes** (GT1,GT2) of the output push-pull transistors. The first transistor (T5) has a threshold voltage equal to or slightly less than that of the output transistor which carries the low signal, e.g. T2. The discharge path via one cross-coupled transistor (T6 or T7) is interrupted by a buffer transistor which receives an inverted clock signal.

As the potential of one output push-pull transistor becomes higher than that of the other, the cross-coupled transistors change states. The parasitic capacitance (C1) discharges to the threshold voltage of the diode-connected transistor (T5), which is identical to that of the output transistors. The diode-connected transistor (T5) becomes non-conducting and the parasitic capacitance (C2) charges to the high level of the (not 5) input signal. If this clock signal becomes low, the inverter (30) will continuously be in a stable state.

ADVANTAGE - Capacitive cross-talk is reduced. Small voltage sweep as control signal is provided.
3a/4
ABEQ EP 141474 B UPAB: 19930925
A digital switching circuit which comprises first (T1) and second (T2) insulated gate field effect transistors, of which **conduction channels** located between main electrodes of the transistors are connected in series between a first (1) and a second (2) supply terminal, the transistors being opposite-wise controllable by logical complementary control signals (S,S
ABEQ US 4642485 A UPAB: 19930925
The digital switching circuit comprises two insulated gate field effect transistors and **conduction channels** located between source and drain electrodes of the transistors being connected in series between two supply terminals in operation the ifrst transistor receiving at its **gate electrode** a control signal and the second transistor receiving at its **gate electrode** a second control such that one of the transistors is rendered conducting and theother transistor is rendered non-conducting.

The first control signal is an inverted version of the second control signal. A switchable clamp characterised in thast the **gate electrodes** of the two transistors are connected to the switchable clamp for keeping the **gate electrode** of only the non-conducting transistor at a voltage level equal to or lower than the threshold voltage of the non-conducting transistor.

ADVANTAGE - Requires smaller voltage sweep as control signal and is insensitive to capacitive cross-talk.

L101 ANSWER 9 OF 32 WPIX (C) 2002 THOMSON DERWENT
AN 1987-336107 [48] WPIX
DNN N1987-251682 DNC C1987-143387
TI Construction of **lateral** pnp-transistors in VLSI-circuits - which have low-current path removed from surface resulting in high gain.
AW SCALE INTEGRATE.
DC L03 U11 U12 U13
IN ARNDT, J
PA (TELE) TELEFUNKEN ELECTRONIC GMBH
CYC 4

PI	EP 247386	A	19871202 (198748)*	DE	11p	
	DE 3618166	A	19871203 (198749)		10p	
	JP 62291171	A	19871217 (198805)			
	US 4829356	A	19890509 (198922)		10p	
	DE 3618166	C	19891026 (198943)			
	US 4956305	A	19900911 (199039)			
	EP 247386	B	19910327 (199113)			
	DE 3768854	G	19910502 (199119)			
	KR 9506479	B1	19950615 (199713)			H01L029-73

ADT EP 247386 A EP 1987-106346 19870502; DE 3618166 A DE 1986-3618166 19860530; JP 62291171 A JP 1987-131977 19870529; US 4829356 A US 1987-46534 19870506; US 4956305 A US 1989-337945 19890414; KR 9506479 B1 KR 1987-5539 19870530
PRAI DE 1986-3618166 19860530
REP 1.Jnl.Ref; A3...8811; EP 100677; EP 152929; JP 55110071; No-SR.Pub; US 4283236
IC H01L021-82; H01L027-06; H01L029-72; H03F003-34
ICM H01L029-73
ICS H01L021-82; H01L027-06; H01L029-72; H03F003-34
AB EP 247386 A UPAB: 19930922
Two p(+)-diffused regions (19c,d) representing emitter and collector are formed adjacent to each other in an n-well, which forms the base-region of the transistor. A buried zone (25) is formed, at a distance from the surface, which is partly **compensated** or just overcompensated by p-type impurities (fig.4) to such a level that no self-conduction between emitter and collector can occur. Although the transistor preferred is PNP the main claim also allows for a **lateral** PNP-transistor.

The buried zone (25) is pref. obtained by implantation, e.g. such as is used to adjust the MOS-device threshold value, occurs at pref. 0.3 micron from the surface and reaches 0.6 micron depth. Its **doping** level is pref. 10 power14 - 10 power16 ats/cm3 of p- or n-type impurities. The surface between emitter and collector (21) is pref. covered with a passivation layer (24), pref. SiO2 or Si3N4, on which an electrode (15d) is formed, pref. of polycrystalline Si, which is shorted to the emitter(23k). The transistor is pref. integrated with CMOS and NPN-bipolar transistors in a single IC.

USE/ADVANTAGE - The transistor shows a gain (B) at currents below 10 micro-amps. which is at least an order of magnitude higher than that of a conventional **lateral** PNP-transistor. It has also a lower noise-level because the charge carriers no longer are scattered by the surface. The transistor can be constructed easily in a process to mfr. CMOS-devices.
1/7
ABEQ DE 3618166 C UPAB: 19930922
PNP **lateral** transition consists of two zones (19c, 19d) forming emitter and collector, in the surface of a semiconductor (12) of a conductivity type, e.g. n type, different from the zones. The region (26) between the zones forms the active base zone and contains a semiconductor zone (25) which contains contradoping imperfections against the remaining region. The minority charge carriers in the base zone are concentrated at a distance from the semiconductor surface, between the emitter zone and the collector zone. The buried semiconductor zone is of the substrate

conductivity type with reduced **doping** compared with the rest of the base zone.

ADVANTAGE - Improved amplifying properties, easy to mfr.

ABEQ EP 247386 B UPAB: 19930922

Lateral p-n-p transistor with, inset into the surface of a semiconductor region (12) of the first conduction type, two zones (19c, 19d) of the second conduction type forming emitter and collector, in which the part of the semiconductor region of the first conduction type lying between these two zones forms the active base zone (26), and in which the active base zone (26) contains below the semiconductor surface and bordering on the emitter and collector zones (19c and 19d) a buried semiconductor zone (25) which compared with the rest of the surrounding region of the active base zone (26) contains additional counterdoping foreign atoms, whereby the minority charge carriers are concentrated in the active base zone (26) at a spacing from the semiconductor surface between the emitter zone (19d) and the collector zone (19c).

ABEQ US 4829356 A UPAB: 19930922

In a **lateral** transistor with emitter and collector regions incorporated into the surface of a semiconductor of a different conductivity type, the region of the semiconductor between the emitter and collector regions forming the active regions which has buried semiconductor zone. The zone extends to the emitter and collector regions and contains additional counter-**doping** impurities relative to the conductivity of the remaining surrounding parts of the active base region. Minority charge carriers in the active base region are thereby concentrated at a distance from the semiconductor surface, between emitter and collector regions.

ADVANTAGE - improved gain properties and easily mfd..

ABEQ US 4956305 A UPAB: 19930922

The pnp **lateral** transistor has two regions of p-type conductivity which are incorporated into the surface of a semiconductor area of n-type conductivity. The two regions constitute the emitter and collector regions. The portion of the semiconductor area of n-type conductivity located between these two regions constitutes the activee base region. The transistor is based on the fact that the active base region includes below the semiconductor surface and adjacent to the emitter region and to the collector region, a buried semiconductor region. This region contains additional counter-**doping** impurities relative to the remaining surrounding base region area. The buried region produces a **conductive channel** for the minority charge carriers in the base region. This reduces the parasitic surface recombination and substrate transistor influences. ADVANTAGE - Has very high direct current gain.

FS CPI EPI

L101 ANSWER 31 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 1971:545251 HCAPLUS
DN 75:145251
TI Irradiation defects and the electrical quality of ion implanted silicon
AU Davies, D. Eirug; Roosild, S.
CS Air Force Cambridge Res. Lab., Air Force Syst. Command, Bedford, Mass., USA
SO Solid-State Electron. (1971), 14(10), 957-83
CODEN: SSELA5
DT Journal
LA English
CC 71 (Electric Phenomena)
AB Ion-irradiated Si that had been annealed to recover the lattice disorder was examd. for residual elec. active defects. To do so, minority carrier lifetimes were monitored by measuring the switching behavior of planar diffused diodes that were damaged with Si or C ions on their lightly **doped side**. Defects stable to temps. well beyond those normally assocd. with lattice disorder annealing are found throughout the investigated dose range of 1012-1015 ions/cm2. With appropriate higher-temp. annealing, the deteriorated lifetime recovers sufficiently so as not to restrict the use of implantation for fabricating devices. The accompanying **compensating** properties expected of these defects also explain many of the features in the manner by which the conductance of B-, P-, and As-implanted layers increase on annealing.
ST ion implanted silicon; radiation defect silicon; defect radiation silicon

L101 ANSWER 32 OF 32 HCAPLUS COPYRIGHT 2002 ACS

AN 1963:716 HCAPLUS

DN 58:716

OREF 58:103a-c

TI Filamentary impact ionization in **compensated** germanium at 4.2.degree.K

AU Melngailis, I.; Milnes, A. G.

CS Carnegie Inst. of Technol., Pittsburgh, PA

SO J. Appl. Phys. (1962), 33, 995-1000

DT Journal

LA Unavailable

CC 9 (Electric and Magnetic Phenomena)

AB An exptl. study is made of filamentary impact ionization breakdown observed in Ge **doped** with both Group III and Group V elements at liquid-He temp. The approx. size of the filament at various current values after ionization is estd. from the measurement of voltage-current characteristics of small cross section bars with high current pulses. Measurements are also made with cylindrical "tecnetron" structures in which the **conduction channel** can be reduced to very small areas by reverse bias of a ring-shaped p-n junction alloyed around a small cylindrical bar. Results of the 2 expts. are consistent. Near the lowest current value at which ionization can be sustained (about 40 .mu.a.), the approx. filament diam. is 10-3 cm.

L101 ANSWER 15 OF 32 JAPIO COPYRIGHT 2002 JPO
AN 1983-170119 JAPIO
TI SEMICONDUCTOR ANALOG SWITCH
IN UENO MASAHIRO; HAMADA KANMAN; SASE TAKASHI; FURUTOKU SHOICHI
PA HITACHI LTD
PI JP 58170119 A 19831006 Showa
AI JP 1982-51107 (JP57051107 Showa) 19820331
PRAI JP 1982-51107 19820331
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 1983
IC ICM H03K017-687
AB PURPOSE: To obtain a semiconductor analog switch which has reduced dependance on the input voltage with small error voltage, by using two switching field effect transistors (TR) having equal **conductive channels** and connected in parallel and a **compensating** field effect transistor having the same conductive type as the switching field effect transistors with the source and the drain short- circuited to each other.
CONSTITUTION: When an analog switch is turned off, i.e. gates G<SB>1</SB> and G<SB>2</SB> are set at 0 and 1 respectively, the channels of the 1st and the 2nd TRs QMN<SB>2</SB> and QMN<SB>2</SB> disappear. Instead a channel is formed under the gate of the 3rd TR QCN<SB>1</SB> for **compensation** whose gate is connected to the 2nd gate terminal which is driven with the polarity opposite to the 1st gate terminal. As the current is set at 0 at a moment when the analog switch is turned off, the carriers within the TRs QMN<SB>1</SB> and QMN<SB>2</SB> are discharged by 1/2 toward the source and drain **sides** respectively and then absorbed almost completely by the channel of the TR QCN<SB>1</SB> and not delivered to the outside of the switch.

L101 ANSWER 18 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:550897 HCAPLUS
DN 131:279894
TI Performance predictions for a silicon velocity modulation transistor
AU Crow, G. C.; Abram, R. A.
CS Physics Department, Durham University, Durham, DH1 SLE, UK
SO International Conference on the Physics of Semiconductors, 24th, Jerusalem, Aug. 2-7, 1998 (1999), Meeting Date 1998, 1844-1847. Editor(s): Gershoni, David. Publisher: World Scientific, Singapore, Singapore.
CODEN: 67YTAU
DT Conference; (computer optical disk)
LA English
CC 76-3 (Electric Phenomena)
AB A Monte Carlo simulation was devised and used to model sub-micron Si velocity modulation transistors, with the intention of designing a terahertz device. The simulated devices have nominal top and back gate lengths of 0.1 .mu.m, and the **conduction channels** have similar thickness. Mobility modulation is achieved by heavily **compensated doping** at one **side** of the channel, and interface roughness. Simulations at T = 77K and 300K suggest that current can be switched between the low and high mobility regions of the channel within 1 ps, but the main obstacle to practical device operation is the small ratio of the steady drain currents for the device operating in the high and low mobility regimes, which decreases with increasing drain-source bias. Such a device should clearly work best when the elec. fields along the channel are small, so that impurity scattering has a significant influence on the electron mobility. In the poster, the performance is compared with that for a short gate dual channel Si/SiGe transistor.
ST Monte Carlo simulation silicon velocity modulation transistors

L101 ANSWER 20 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:22246 HCAPLUS
DN 130:161320
TI Performance predictions for a silicon velocity modulation transistor
AU Crow, G. C.; Abram, R. A.
CS Department of Physics, University of Durham, South Road, Durham, DH1 3LE, UK
SO Journal of Applied Physics (1999), 85(2), 1196-1202
CODEN: JAPIAU; ISSN: 0021-8979
PB American Institute of Physics
DT Journal
LA English
CC 76-3 (Electric Phenomena)
AB A Monte Carlo simulation was devised and used to model submicron Si velocity modulation transistors with the intention of designing a picosecond switch. The simulated devices have nominal top and back gate lengths of 0.1 .mu.m, and the **conduction channels** have similar thickness. Mobility modulation has so far been achieved by heavily **compensated doping** and interface roughness at one **side** of the channel. The simulated devices have a high intrinsic speed; simulations performed for T = 77 K suggest that current can be switched between the low and high mobility regions of the channel within 1.5 ps. However, in unstrained Si devices the main obstacle to practical device operation is the rather small current modulation factor (the ratio of the steady drain currents for the device operating in the high and low mobility regimes), which decreases towards unity with increasing drain-source bias. Such a device should work best for small elec. fields along the channel (.apprx.105 V m-1), the regime where impurity scattering has its greatest influence on the electron mobility.
ST Monte Carlo simulation silicon velocity modulation transistor
IT Simulation and Modeling, physicochemical

L101 ANSWER 21 OF 32 HCAPLUS
AN 1997:751075 HCAPLUS
DN 128:69131
TI Modification of the 2D electronic properties in Si-.delta.-**doped** InSb due to surface effects
AU De Keyser, A.; Bogaerts, R.; Van Bockstal, L.; Herlach, F.; Karavolas, V. C.; Peeters, F. M.; Van De Graaf, W.; Borghs, G.
CS Laboratorium voor Vaste-Stoffysica en Magnetisme, Katholieke Universiteit Leuven, Louvain, B-3001, Belg.
SO High Magnetic Fields in the Physics of Semiconductors II, International Conference, 12th, Wuerzburg, Germany, July 29-Aug. 2, 1996 (1997), Meeting Date 1996, Volume 1, 383-386. Editor(s): Landwehr, G.; Ossau, W. Publisher: World Scientific, Singapore, Singapore.
CODEN: 65IGAX
DT Conference
LA English
CC 76-3 (Electric Phenomena)
AB A magnetotransport study of single Si-.delta.-layers in InSb has been performed in order to investigate the characteristics of the two-dimensional **conduction channel** in these structures as a function of the distance between the .delta.-layer and the sample surface. When the .delta.-layer is positioned close to the surface, the transport properties show little sensitivity to the **doping** characteristics. The transport can be described in terms of a two-dimensional electron gas (2DEG) in the delta-layer with a small contribution from bulk electrons. If the .delta.-layer is placed further away from the surface, the transport properties change drastically. Plateau-like features in .rho.xx are accompanied by very strong oscillatory behavior in .rho.xy. This shows a strong resemblance to the effects obsd. in nearly **compensated** GaSb-InAs quantum wells where two-dimensional electrons and holes form parallel **conduction channels**.
ST electronic property silicon **doped** indium antimonide
IT **Doping**

L101 ANSWER 24 OF 32 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:928016 HCAPLUS
DN 124:18923
TI The effect of organometallic vapor phase epitaxial growth conditions on wurtzite GaN electron transport properties
AU Gaskill, D. K.; Wickenden, A. E.; Doverspike, K.; Tadayon, B.; Rowland, L. B.
CS Lab. Advanced Material Synthesis, Naval Res. Laboratory, Washington, DC, 20375, USA
SO Journal of Electronic Materials (1995), 24(11), 1525-30
CODEN: JECMA5; ISSN: 0361-5235
PB Minerals, Metals & Materials Society
DT Journal
LA English
CC 76-1 (Electric Phenomena)
Section cross-reference(s): 75
AB The growth issues known to effect the quality of GaN organometallic vapor phase epitaxial films are reviewed and the best 300K mobility vs. electron concn. data are discussed. The data probably represent transport properties intrinsic to films grown on sapphire. From the results of Hall measurements, the unintentional donor in high quality GaN films cannot be Si since the donor ionization energy is much larger than that of films intentionally **doped** with Si (36 vs. 26 meV). Elec. properties of a **doped** channel layer are shown not to be significantly different from those of thick films which implies a viable technol. for **conducting channel** devices. It is argued that 77K Hall measurements are a useful indicator of GaN film quality and a compilation of unintentionally and Si **doped** data is presented. The 77K data imply that, at least over a limited range, Si-**doping** does not appreciably change the **compensation** of the GaN. The 77K data indicate that the low mobilities of films grown at low temps. are probably not related to **dopant** impurities.

25/9/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6990715 INSPEC Abstract Number: B2001-09-2560R-012
Title: Four-**terminal** poly-Si TFTs with improved reliability
Author(s): Park, C.-M.; Jeon, J.-H.; Yoo, J.-S.; Han, M.-K.
Author Affiliation: Seoul Nat. Univ., South Korea
Conference Title: Society for Information Display 1999 International Symposium p.394-7
Publisher: Soc. Inf. Display (SID), Santa Ana, CA, USA
Publication Date: 1999 Country of Publication: USA CD-ROM pp.
Material Identity Number: XX-1999-01213
Conference Title: Proceedings of the 1999 SID International Symposium, Seminar & Exhibition
Conference Date: 18-20 May 1999 Conference Location: San Jose, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Applications (A); New Developments (N); Practical (P)
Abstract: We fabricated a novel poly-Si TFT, which employs a counter-**doped lateral** body **terminal** in order to suppress kink effects and improve the device stability. The device also employs a buried **channel** , which increase on-current and operating frequency. The proposed poly-Si TFT exhibits superb dynamic reliability compared to conventional poly-Si TFTs after AC stress. (3 Refs)
Subfile: B
Descriptors: buried layers; CMOS integrated circuits; doping profiles; elemental semiconductors; liquid crystal displays; MOSFET; semiconductor

25/9/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

6761697 INSPEC Abstract Number: B2000-12-7260F-038
Title: A novel four **terminal** poly-Si TFT suppressing kink and improving reliability
Author(s): Cheol-Min Park; Ji-Hoon Kang; Kee-Chan Park; Min-Koo Han
Author Affiliation: Sch. of Electr. Eng., Seoul Nat. Univ., South Korea
Conference Title: Flat-Panel Displays and Sensors - Principles, Materials and Processes. Symposium (Materials Research Society Symposium Proceedings Vol.558) p.357-62
Editor(s): Chalamala, B.R.; Friend, R.H.; Jackson, T.N.; Libsch, F.R.
Publisher: Mater. Res. Soc, Warrendale, PA, USA
Publication Date: 2000 Country of Publication: USA xv+615 pp.
ISBN: 1 55899 465 3 Material Identity Number: XX-2000-01520
Conference Title: Flat-Panel Displays and Sensors - Principles, Materials and Processes. Symposium
Conference Date: 4-9 April 1999 Conference Location: San Francisco, CA, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Experimental (X)
Abstract: We fabricated a new device, which employs counter-**doped** **lateral** body **terminal** (CLBT) in order to suppress kink effects and improve the device stability. The proposed device also employs a buried **channel** (BC), which increases ON-current and operating frequency. Although LDD structure is not employed in the proposed device, low OFF-current is successfully obtained due to elimination of minority carrier through CLBT. We have measured the dynamic properties of poly-Si TFT device and circuit. The reliability of TFT and circuits after AC stress is also discussed. The proposed poly-Si TFT has high ON-current and low OFF-current compared with conventional 3-**terminal** poly-Si TFT. The 4-**terminal** device characteristics were measured with source and CLBT shorted. The proposed device exhibits superior performance to conventional device in ON-current because BC prevents carrier scattering to gate oxide. We have performed bias and high temperature stress test of ring oscillator in order to investigate dynamic reliability between conventional poly-Si TFT and proposed 4-**terminal** poly-Si TFT. Our experimental results show that BC enables the device to have high mobility and switching frequency (33 MHz at V/sub DD/=15 V). The minority carrier elimination of CLBT suppresses kink effects and makes superb dynamic reliability of CMOS circuit. (5 Refs)
Subfile: B
Descriptors: buried layers; driver circuits; elemental semiconductors; ion implantation; laser beam annealing; liquid crystal displays;

25/9/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

6579568 INSPEC Abstract Number: B2000-06-2560R-013
Title: The fabrication of four-**terminal** poly-Si TFTs with buried **channel**
Author(s): Sang-Hoon Jung; Cheol-Min Park; Juhn-Suk Yoo; Hyoung-Bae Choi; Min-Koo Han
Journal: Transactions of the Korean Institute of Electrical Engineers, C
vol.48, no.12 p.761-7
Publisher: Korean Inst. Electr. Eng,
Publication Date: Dec. 1999 Country of Publication: South Korea
CODEN: CHNODD ISSN: 1229-246X
SICI: 1229-246X(199912)48:12L.761:FFTP;1-6
Material Identity Number: H331-2000-002
Language: Korean Document Type: Journal Paper (JP)
Treatment: New Developments (N); Practical (P); Experimental (X)
Abstract: Poly-Si TFTs (polycrystalline silicon thin film transistors) fabricated on a low cost glass substrate have attracted a considerable amount of attention for pixel elements and peripheral driving circuits in AMLCD (active matrix liquid crystal display). In order to apply poly-Si TFTs for high resolution AMLCD, a high operating frequency and reliable circuit performances are desired. A new poly-Si TFT with CLBT (counter **doped lateral** body **terminal**) is proposed and fabricated to suppress kink effects and to improve the device stability. This proposed device with BC (buried **channel**) is fabricated to increase ON-current and operating frequency. Although the troublesome LDD structure is not used in the proposed device, a low OFF-current is successfully obtained by removing the minority carrier through the CLBT. We have measured the dynamic properties of the poly-Si TFT device and its circuit. The reliability of the TFTs and their circuits after AC stress are also discussed in our paper. Our experimental results show that the BC enables the device to have high mobility and switching frequency (33 MHz at V/sub DD/=15 V). The minority carrier elimination of the CLBT suppresses kink effects and makes for dynamic reliability of the CMOS circuit. We have analyzed the mechanism in order to see why the ring oscillators do not operate by analyzing AC stressed device characteristics. (9 Refs)
Subfile: B
Descriptors: carrier mobility; driver circuits; elemental semiconductors;

25/9/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

04230551 INSPEC Abstract Number: B9210-2570D-015
Title: Process and device simulation in designing thin film CMOS/SOI technology
Author(s): Spencer, O.S.; Seliskar, J.; Wang, L.K.; Haddad, N.F.
Author Affiliation: IBM Federal Sector Div., Manassas, VA, USA
Conference Title: 1991 IEEE International SOI Conference Proceedings (Cat. No.91CH3053-6) p.82-3
Publisher: IEEE, New York, NY, USA
Publication Date: 1991 Country of Publication: USA xxii+183 pp.
ISBN: 0 7803 0184 6
U.S. Copyright Clearance Center Code: 0 7803 0184 6/91$01.00
Conference Sponsor: IEEE
Conference Date: 1-3 Oct. 1991 Conference Location: Vail Valley, CO, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: The authors report on process modeling used FEDSS (Finite Element Diffusion Simulation System) together with device modeling using FIELDAY (FInite ELement Device AnalYsis) to analyze fully depleted thin film SOI (silicon-on-insulator) processes/devices. The FEDSS output after simulating drain implantation is presented, showing drain profile and polysilicon **side wall** oxides. **Channel doping** for both p- and n-type devices was p-type, and FEDSS modeling from process parameters found the device **channel** doping to be 8*10/sup 15//cm/sup 3/, tailing off in the 100 AA gate surface 6*10/sup 15//cm/sup 3/ due to boron depletion. Measured results for the n-**channel** device were compared with the FIELDAY simulations. The difference between calculation and measurements increases for higher gate voltages. After the DC **terminal** characteristics were reconciled, the breakdown characteristics of the models were investigated. (4 Refs)
Subfile: B
Descriptors: CMOS integrated circuits; electric breakdown of solids; finite element analysis; integrated circuit technology; semiconductor

25/9/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

01914365 INSPEC Abstract Number: B82046574
Title: An area-variable MOS varicap and its application in programmable TAP weighting of CCD transversal filters
Author(s): Bhattacharyya, A.B.; Wallinga, H.
Author Affiliation: Centre for Appl. Res. in Electronics, Indian Inst. of Technol., Hauz Khas, New Delhi, India
Journal: IEEE Transactions on Electron Devices vol.ED-29, no.5 p. 827-33
Publication Date: May 1982 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
Language: English Document Type: Journal Paper (JP)
Treatment: Applications (A); New Developments (N); Practical (P)
Abstract: A new three-**terminal** MOS varicap is proposed where the **terminal** capacitors are made voltage variable not by the modulation of depletion width but by changing the area of inversion under the gate. An MOS capacitor realized on silicon with an impurity gradient along the surface provides the control on the area of inversion because the gate threshold voltage is determined by the doping concentration at the surface. The inhomogeneous doping along the surface is implemented making use of the **lateral** diffusion from a **doped** oxide surface. Fabrication details of the capacitor compatible with n-**channel** silicon gate technology are presented. The C-V relationship for the **terminal** capacitors is simulated by a piecewise model and agreement with the measured results is shown. The Area-Variable MOS Varicap (AVMOSV) is used in implementing an electrically programmable CCD filter with variable TAP weighting. Computer simulation shows considerable promise of area-variable capacitors in TAP weight control and transversal filter realization. Preliminary performance characteristics of a programmable CCD filter are presented. (13 Refs)
Subfile: B
Descriptors: active filters; capacitors; charge-coupled device circuits;

18/9/2 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

0939063 NTIS Accession Number: AD-D009 048/0/XAB
Planar **Doped** Barrier Gate Field Effect Transistor
(Patent Application)
Malik, R. J. ; AuCoin, T. R.
Department of the Army, Washington, DC.
Corp. Source Codes: 000137000; 109900
Report No.: PAT-APPL-6-323 858
Filed 23 Nov 81 11p
Languages: English Document Type: Patent
Journal Announcement: GRAI8208

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NTIS Prices: PC A02/MF A01
Country of Publication: United States

Disclosed is an epilayer field effect transitor having a planar **doped** barrier gate formed on an n-type semiconductor planar channeel region intermittent drain and source terminals formed on the surface of the **channel region**. The semiconductor **channel region** is fabricated on a semiconductor substrate, preferably GaAs and being separated therefrom by one or more semiconductor planar buffer regions. The planar **doped** barrier gate comprises an n+ - pi - p(+) - pi structure grown by molecular beam epitaxy over the n-type **channel region**. Application of an electrical potential to the gate modulates the **channel charge** depletion in the semiconductor **channel region** underlying the gate causing a variation in the **channel conductance laterally** between the source and drain terminals. (Author)

20/9/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

5432763 INSPEC Abstract Number: B9701-2560S-011
Title: A **lateral** bipolar-mode field effect transistor using SOI substrate
Author(s): Seong-Dong Kim; Moo-Sup Lim; Jae-Hyung Kim; Min-Koo Han; Yeam-Ik Choi
Journal: Transactions of the Korean Institute of Electrical Engineers vol.45, no.7 p.990-6
Publisher: Korean Inst. Electr. Eng,
Publication Date: July 1996 Country of Publication: South Korea
CODEN: CHNODD ISSN: 0254-4172
SICI: 0254-4172(199607)45:7L.990:LBMF;1-9
Material Identity Number: C896-96011
Language: Korean Document Type: Journal Paper (JP)
Treatment: New Developments (N); Practical (P)
Abstract: A new **lateral** SOI bipolar mode field-effect transistor (BMFET) is proposed and verified by numerical simulation and experiments. The device has a **lateral** JFET structure providing a **lateral** **channel** between the buried oxide and p/sup +/ gate junction. The minority carrier injection from the gate causes a high current operation with a very low saturation voltage due to the **conductivity** modulation effect in the high-resistivity drift region. It is shown that the normally-off characteristics and the current gain are changed by the potential barrier in the **channel region** which is controlled by the **channel** depth and length, the buried oxide thickness, the substrate **dopant** type and the **doping** concentration of n drift region. Higher breakdown voltage and larger current gain in the range of high drain current are obtained by introducing a low-resistivity n layer in the drift region employing the RESURF principle that the surface electric field is minimized when the implantation dose of the drift region is around 10/sup 12/ cm/sup -2/. (10 Refs)
Subfile: B

/9/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

02519726 INSPEC Abstract Number: B85050476
Title: Modeling of polysilicon resistors, p-n junction diodes and MOSFETs
Author(s): Khondker, A.N.; Ahmed, S.S.; Liou, T.; Kim, D.M.
Author Affiliation: Dept. of Electr. & Comput. Eng., Clarkson Coll., Potsdam, NY, USA
Conference Title: Comparison of Thin Film Transistor and SOI Technologies Symposium p.207-12
Editor(s): Lam, H.W.; Thompson, M.J.
Publisher: North-Holland, New York, NY, USA
Publication Date: 1984 Country of Publication: USA xv+321 pp.
ISBN: 0 444 00899 3
Conference Date: 26-28 Feb. 1984 Conference Location: Albuquerque, NM, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: **Conductivity** in bulk polysilicon is discussed, applicable over a wide range of **dopant** concentration, temperature, grain size and trap density. The I-V behavior in a **lateral** poly p-n junction is analytically modeled, incorporating the effects of carrier lifetime operative in crystalline grain and amorphous **conducting** boundaries. In particular, the extremely short carrier lifetime within the grain boundary is shown to provide an ohmic **conduction channel** in a direction parallel to current flow. This ohmic current can account for the unusually high current levels observed at small applied voltages. Also, the shift of the threshold voltage of MOS devices, as influenced by grain traps near the **channel region**, is analysed. (15 Refs)
Subfile: B
Descriptors: carrier lifetime; grain boundaries; insulated gate field

20/9/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

00817660 INSPEC Abstract Number: B75037543
Title: **Lateral** transistors as active guard ring in FET circuits
Author(s): Clemen, R.; Haug, W.; Schnadt, R.
Author Affiliation: IBM, Armonk, NY, USA
Journal: IBM Technical Disclosure Bulletin vol.18, no.2 p.440-1
Publication Date: July 1975 Country of Publication: USA
CODEN: IBMTAA ISSN: 0018-8689
Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: The ever increasing use of bootstrap circuits (capacitive feedback) in integrated circuits leads to a frequency recurring problem, for example, in N-**channel** technology: An N/sup +/ **doped** region is discharged to approximately OV. An adjacent line is switched from the positive supply voltage to O V. The bootstrap capacity transfers this negative voltage transition to the N/sup +/ **doped** region causing it to adopt a strongly negative potential. If this potential drops below the substrate bias, the N/sup +/ region injects electrons into the P substrate, i.e., the P/N/sup +/ diode is forward biased. To eliminate these difficulties, it is proposed that the jeopardized **doped** region be surrounded by a protective **doped** region of the same **conductivity type**, so that in N-**channel** technology a **lateral** NPN and in P-**channel** technology a **lateral** PNP transistor is formed, across which the spurious injection current is extracted. (0 Refs)

20/9/7 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

2053653 NTIS Accession Number: AD-A335 240/8/XAB
SiC Discrete Power Devices-Analysis and Optimization of the Planar 6H-SiC ACCUFET; A Planar **Lateral Channel** SiC Vertical High Power JFET; The Planar **Lateral Channel** MESFET-A New SiC Vertical Power Device; Growth via Hot **Wall** Chemical Vapor Deposition Characterization of 6H and 4H SiC Thin Films
(Annual technical rept.15 Jan 97-15 Jan 98)
Davis, R. F. ; Baliga, B. J. ; Tomozawa, H. S. ; Shenoy, P. M.
North Carolina State Univ. at Raleigh.
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Country of Publication: United States
Contract No.: N00014-96-1-0363-1

A novel planar accumulation **channel** SiC MOSFET structure is reported. The problems of gate oxide rupture and poor **channel conductance** previously reported in SiC UMOSFETs are solved by using a buried P+ layer to shield the **channel region**. The fabricated 6H-SiC unterminated devices had a blocking voltage of 350 V with a specific on-resistance of 18 m ohms-sq cm at room temperature for a gate bias of only 5 V. This measured specific on-resistance is within 2.5X of the value calculated for the epitaxial drift region (10(exp 16) /cucm, 10 micrometers), which is capable of supporting 1500 V. In addition, a novel planar **lateral channel** SiC high power JFET is described. Two-dimensional numerical simulations predicted low on-resistances with excellent current saturation and square FBSOA, which have been experimentally confirmed. A novel planar **lateral channel** SiC MESFET structure with vertical current flow in the drift region is also proposed and demonstrated by modeling and fabrication. A hot **wall** chemical vapor deposition system has been constructed for the growth and **doping** of 6H- and 4H-SiC thin films at very high temperatures and high growth rates. The design incorporates a separate load lock to which a growth chamber and a RHEED chamber are attached.

Descriptors: Field effect transistors; *Silicon carbides; *Mosfet semiconductors; High power; **Conductivity**; Two dimensional; High